repair notes on the KEPCO BOP100-1M and the SNQ488-1/2 GPIB cable

- you can find operating and service manuals for the **BOP50-2** devices on the internet, but there are no **BOP100-1M** PDFs available and KEPCO still wants $100 for them
- there is also no pinout for the **SNQ488-1/2** cable needed for the **BIT488-B/D** option
- the BOP50-2 documentation mostly also applies to the BOP100-1, but the power stage is very different.

BOP100-1:

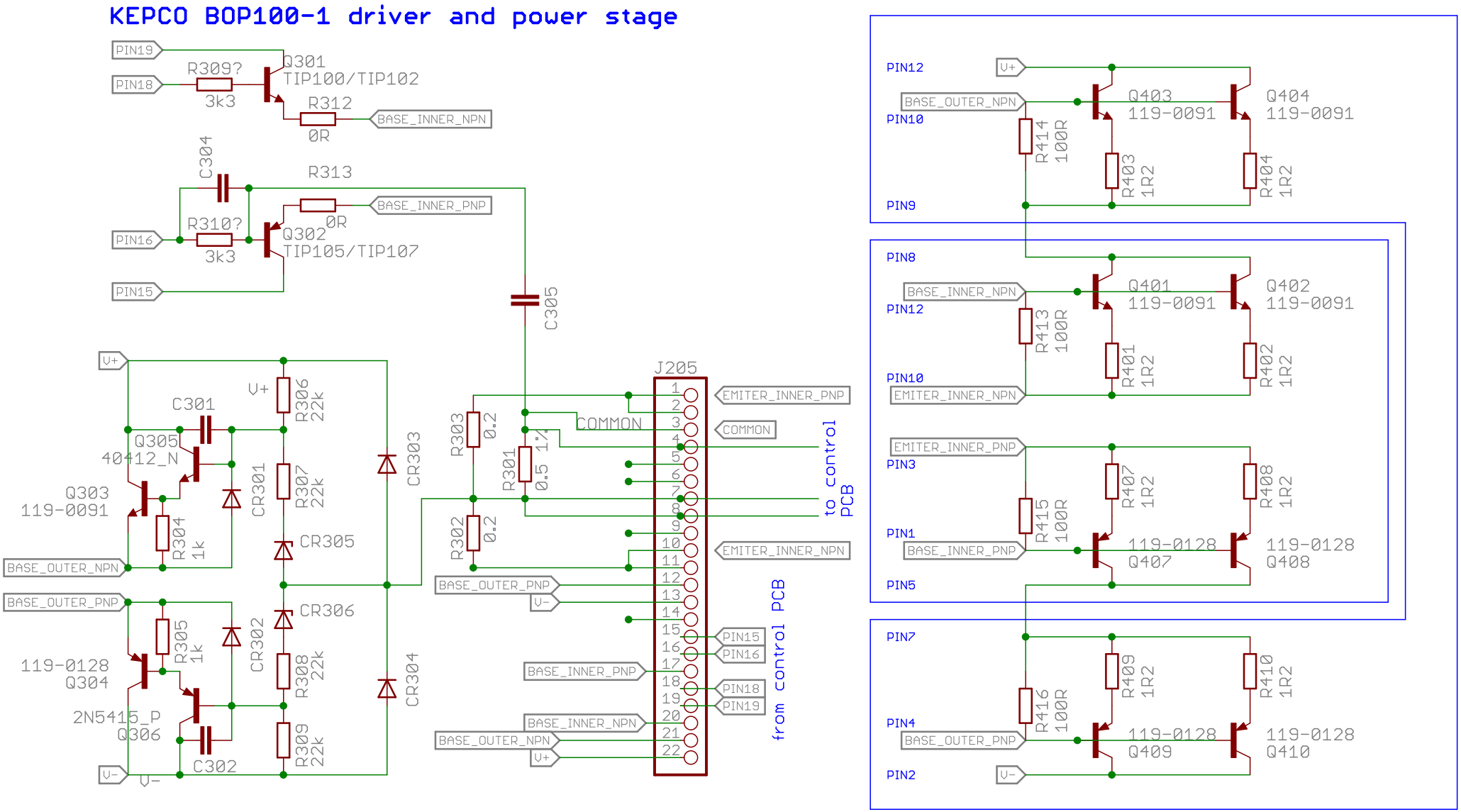
- I have drawn the schematics for the driver board and the power transistor PCBs, there is one version with the connector pins noted and one that is redrawn to be easier to understand
- on my unit I replaced all the power transistors with **MJ15003 / MJ15004** and the drivers stage transistors **Q301 / Q302** with **TIP102 / TIP107**
- my unit did not come with the **PC-15** plug that defines the default configuration, I made my own from a 50-pin 0.1” card edge connector, but I did **not** connect **pin 26 to pin 36**!
- US patent **4004155** describes the general idea of the bipolar power supply, using the the earlier tube driven version
- US patent **4207475** describes the control loop for the bipolar power stage, I have noted the IC numbers and connector pins as found on the main board, also the resistor values given in the **‘475** patent are more or less exactly the same as they are used on the main board. IC18A (57 in the patent) negative bias (59) is derived from the -10V supply using a resistor divider.

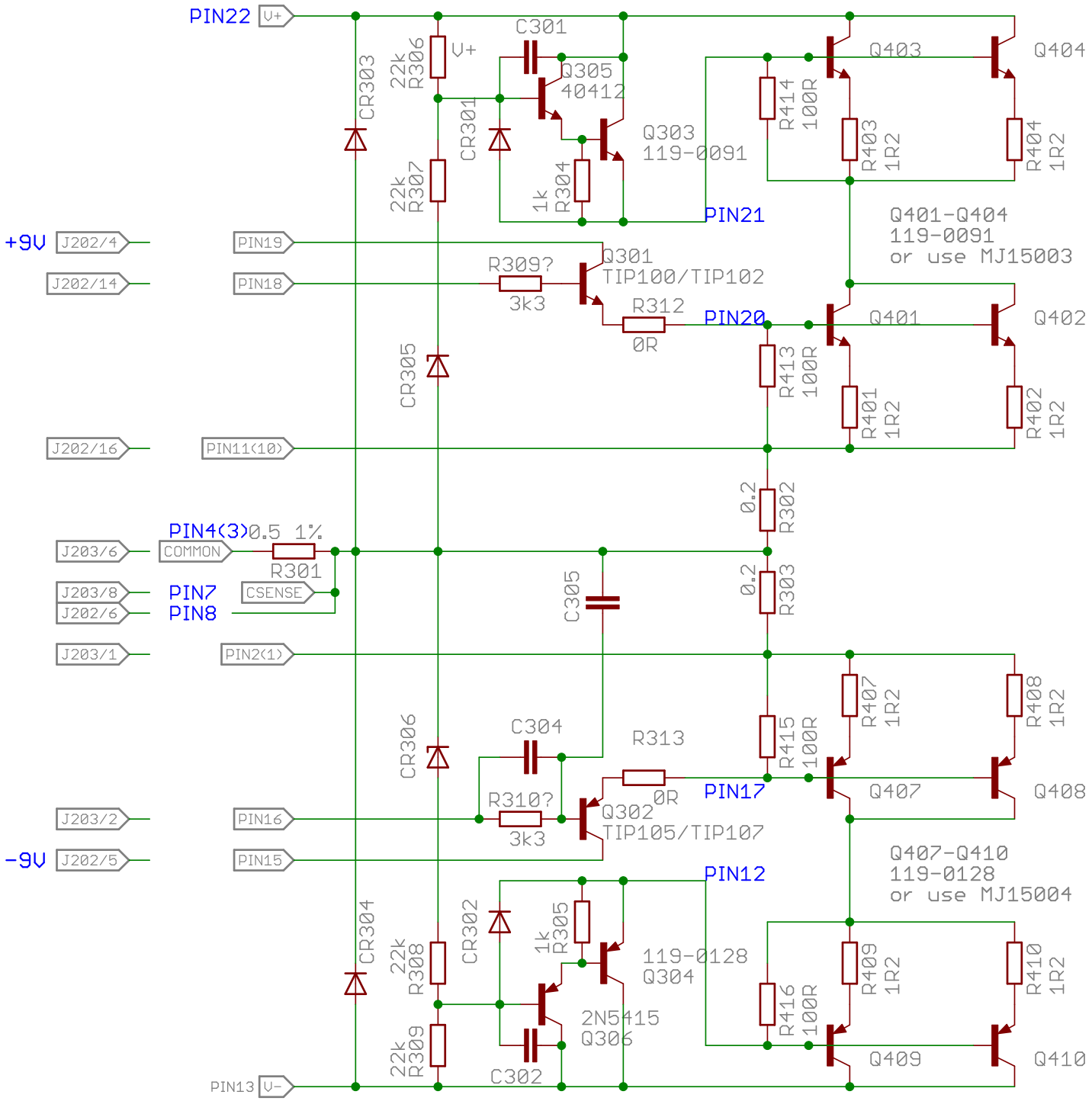
SNQ488-1/2 for BIT 488-B, BIT 488-D cards:

- US patent **4335445** more or less describes the IEE488 card for the **BOP100-1M**
- I have made an adapter PCB that converts from a 24pin GPIB connector to the 2x12 pin card edge connector on the BOP
- **BIT488/500** instruction manual: https://www.kepcopower.com/support/bit488-500.pdf
- **SN488/500 service manual**, very similar to the **BIT488/500**: https://www.artisantg.com/info/Kepco_SN_488_122_Manual_2019115134625.pdf?srsltid=AfmBOoo_ATTdhQF7CH4lTQpCzIMTU0KXG1_Jew1GYG2LBXZZleP8UcrK
- SNQ488-1 cable: https://www.kepcopower.com/support/snq488-2.pdf
- simple C code to program the BIT488-D (BCD) card using linux-gpib: https://github.com/av500/gpib_scripts/blob/main/tools/bop.c
- see also: https://www.thingiverse.com/thing:5988940

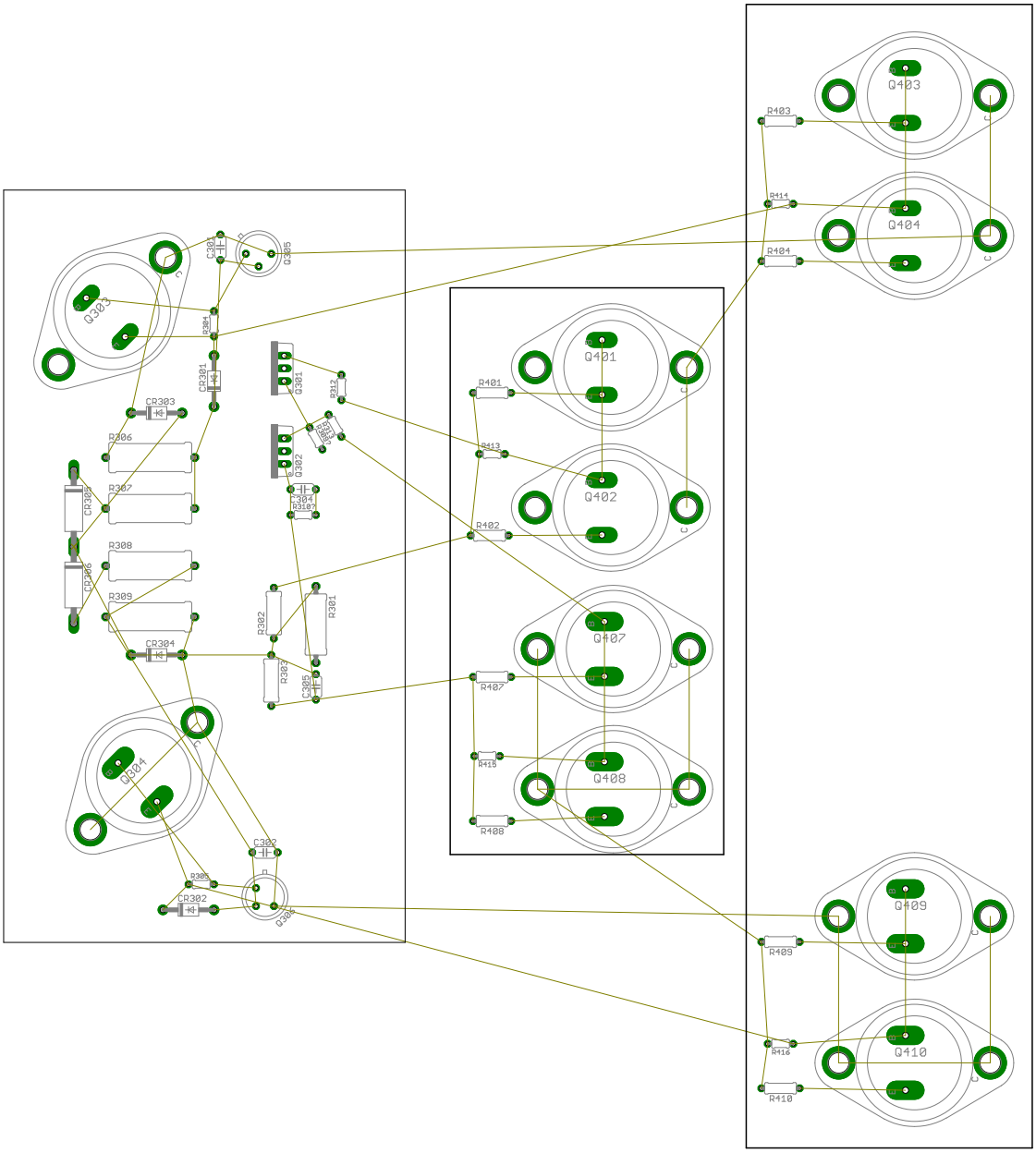
July 2025, Vladimir Pantelic, vpme.de (av500)

KEPCO BOP100-1 driver and power stage





KEPCO BOP100-1 driver and power stage redrawn



KEPCO BOP100-1 driver and power stage
rough component placing

KEPCO MODEL PC-15 MATING CONNECTOR (WIRED, FOR BOP 100-400W MODELS)

DESCRIPTION: The Kepco Model PC-15 is a 50 terminal connector, equipped with cable shell, cable clamp and locking screws. The PC-15 is designed to provide the correct termination for local (front panel) control of Kepco BOP 100W, BOP 200W and BOP 400W Models.

INSTALLATION

1) Unpack the Model PC-15 connector from the polyethylene bag.
2) Mate connector with the BOP rear edge connector.
3) Secure Model PC-15 connector to the chassis of the BOP by engaging and hand-tightening the two knurled fastening screws.

MECHANICAL OUTLINE DRAWING: Refer to FIG. 2 (reverse side).

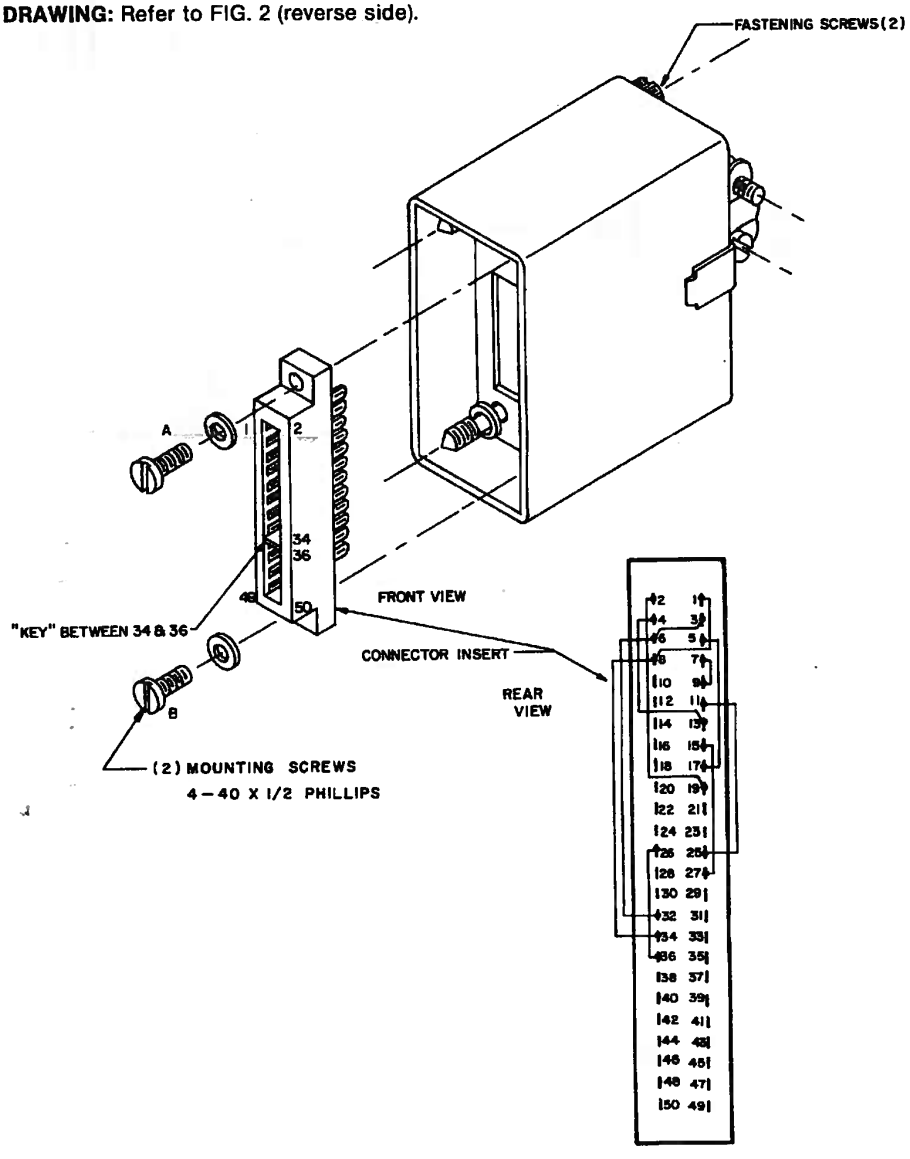


FIG. 1 DISASSEMBLED VIEW OF THE PC-15 MATING CONNECTOR.

United States Patent [19]

Nercessian

[11] **4,207,475**

[45] **Jun. 10, 1980**

[54] **EFFICIENT BIPOLAR REGULATED POWER SUPPLY**

[75] Inventor: **Sarkis Nercessian**, Flushing, N.Y.

[73] Assignee: **Kepco, Inc.**, Flushing, N.Y.

[21] Appl. No.: **929,308**

[22] Filed: **Jul. 31, 1978**

[51] **Int. Cl.**[2] **G05F 1/56**

[52] **U.S. Cl.** **307/52**; 307/77; 323/20; 323/25

[58] **Field of Search** 307/52-55, 307/60, 61, 77; 323/20, 23, 25, 40; 363/131, 133, 134

[56] **References Cited**

U.S. PATENT DOCUMENTS

3,466,455	9/1969	Hecht et al.	323/25 X
3,697,862	10/1972	Taylor	323/20 X
3,935,529	1/1976	Kalmanash et al.	307/52 X
4,004,155	1/1977	Nercessian	307/52

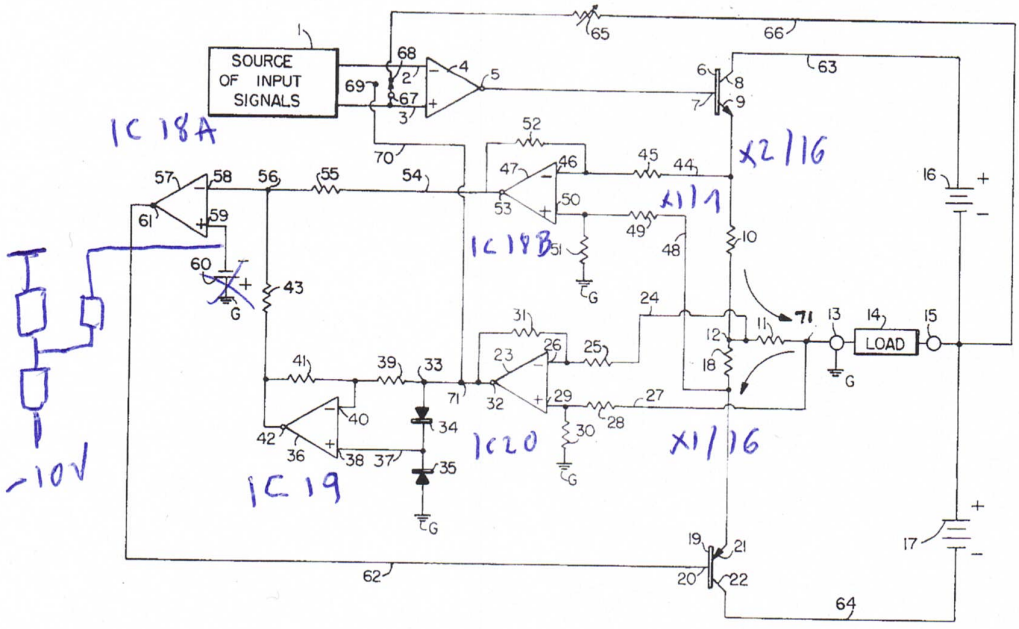
Primary Examiner—A. D. Pellinen

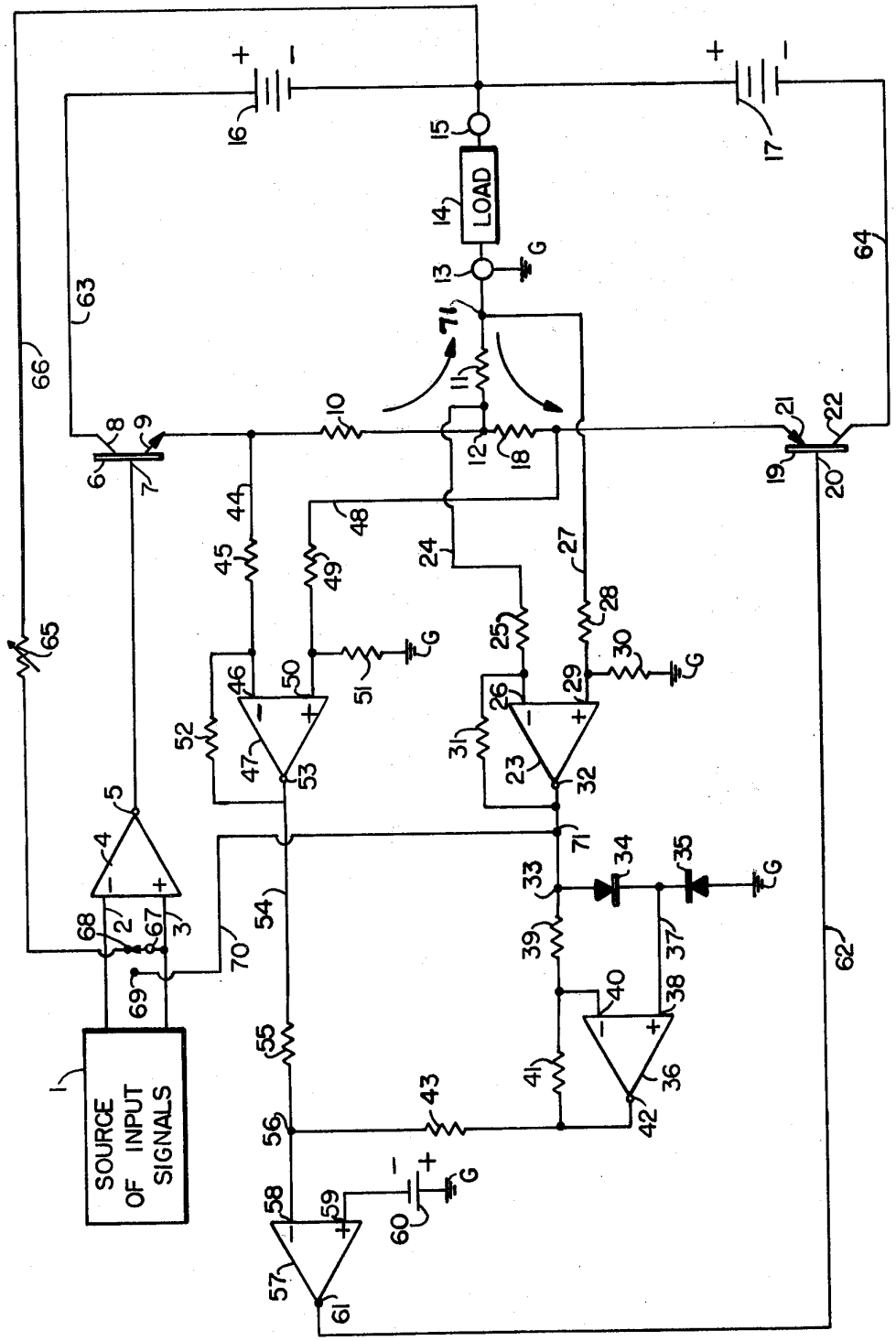
Attorney, Agent, or Firm—Alfred W. Barber

[57] **ABSTRACT**

In a bipolar regulated power supply, two pass devices (transistors) are connected in a complementary symmetry circuit, one controlling the current from a positive voltage source and the other the current from a negative voltage source. One pass device connected in a first control loop is controlled by a source of input signals and feedback from the output terminal. A second control loop maintains a constant quiescent current in the two pass devices. In order to maintain this quiescent current in the presence of load current, a second feedback to the second loop, sensing load current, is provided.

3 Claims, 1 Drawing Figure




SOURCE OF INPUT SIGNALS
LOAD
G

EFFICIENT BIPOLAR REGULATED POWER SUPPLY

PRIOR ART

The prior art is well represented by U.S. Pat. No. 4,004,155 in which two control elements (tubes or transistors) are connected across a load. One of these control elements is set to pass a constant current through the load equal to at least the maximum current to be programmed. The second control element is controlled by an input signal and must be capable of passing at least twice the maximum current to be programmed through the load. The actual load current is the difference between the steady current passed by the first control element and the signal controlled current passed by the second control element.

While the above described system operates well to pass a desired bipolar current through the load, it is rather inefficient. For example, in order to provide zero current through the load each pass element must carry a current equal to the maximum current to, be programmed. At maximum load current in one direction one control element must pass maximum current and the second control element must pass zero current. However, in order to pass maximum current in the other direction, one control element must pass this maximum current while the other must pass double this current.

PRESENT INVENTION

In accordance with the present invention two pass transistors of opposite polarity are connected in series with a source of positive voltage and a source of negative voltage and a common load so that bipolar voltage and current can be programmed to the load through the use of a first degenerative control loop. The second control loop employs two feedbacks. The first feedback includes two current sensing resistors, one in series with each of the pass transistors. One of the pass transistors is controlled by a source of input signals while the other pass transistor is controlled by the second control loop in such a way that with no current supplied to the load, the currents through the two pass transistors are equal and opposite. These currents may be considered as quiescent currents for the purpose of eliminating cross-over distortion in bipolar operation.

The second feedback comes into play when current is passed through the load. Load current is sensed and the resulting voltage drop is amplified and unidirectionalized. This resulting voltage is added to the control voltage going to the second transistor so that its current level is raised in keeping with the demands of the input signal to the first pass transistor. Thus, when current is passed through the load, appropriate current is available from both pass transistors.

The advantage over the prior art is a substantial increase in efficiency in all modes of operation. At the same time quiescent current is supplied eliminating cross-over distortion.

Provision is made for operating the regulator either in voltage or current control mode.

The Drawing is a simplified block diagram of the preferred form of the invention.

The primary circuit on first loop includes a source of input signals **1** (bipolar) applied to inverting input **2** and noninverting input **3** of operational amplifier **4** the output **5** of which is coupled to base **7** of first pass transistor **6**. Collector **8** of pass transistor **6** is connected to a suitable source of positive voltage represented by battery **16** over lead **63**. The emitter **9** of pass transistor **6** is connected through a first current sensing resistor **10** to junction point **12**. The negative half of the circuit comprises transistor **19** having its emitter **21** connected through a second current sensing resistor **18** also to junction point **12**. The collector **22** of pass transistor **19** is connected to a suitable source of negative voltage represented by battery **17** over lead **64**. Base **20** of transistor **19** receives its signals over lead **62** in a manner to be described in detail below. The negative side of positive voltage source **16** and the positive side of negative voltage source **17** are joined and connected to load terminal **15**. The load **14** is connected between load terminals **13** and **15**. Load terminal **13** is connected to ground G, the common of the system. Common terminal **13** is connected through current sensing resistor **11** to junction point **12**. Voltage feedback is taken from load terminal **15** over lead **66**, through gain control resistor **65** to terminal **68** of switch **67-68-69**. The common terminal **67** is connected to noninverting input **3** of operational amplifier **4**. Disregarding for the moment the base control of pass transistor **19**, the primary circuit just described is a complementary symmetry bipolar control circuit including degenerative feedback. The reason the feedback is connected to the non-inverting input of operational amplifier **4** is that there is phase reversal in the positive pass transistor **6** at the feedback point **15**.

The unique operation of the circuitry of the present invention depends on a second current sensing feedback loop. This second loop is mainly responsible for the establishment of a quiescent current in both the positive and negative pass transistors. The voltage drop across the two current sensing resistors **10** and **18** over leads **44** and **48** and through input resistors **45** and **49** is applied to inverting input **46** and non-inverting input **50** respectively of operational amplifier **47**. The gain applied to these voltages at the output of amplifier **47** at output terminal **53** is predetermined by feedback resistor **52** and input shunt resistor **51**. This voltage at output terminal **53** on line **54** through resistor **55** is applied to inverting input **58** of operational amplifier **57**. A predetermined reference voltage represented by battery **60** is applied between ground G and non-inverting input terminal **59**. The amplified difference voltage between that applied to terminal **58** and the reference voltage applied to terminal **59** appears at output terminal **61** and is applied over lead **62** to base **20** of negative voltage pass transistor **19**. This loop causes negative voltage pass transistor **19** to pass a current through its current sensing resistor **18** equal to that passed through current sensing resistor **10** by positive voltage pass transistor **6** when no current is being supplied to load **14**. This may be considered the quiescent current.

As a typical example, the following values of the various resistors provides a quiescent current of 220 milliamperes:

resistor **10**=0.2 ohm
resistor **18**=0.2 ohm
resistor **45**=1.1K ohms
resistor **52**=2.74K ohms
resistor **49**=1.1K ohms
resistor **51**=2.74K ohms
resistor **55**=1K ohms
resistor **43**=10K ohms

reference voltage **60**=0.2 volt

The second control loop includes a second feedback which serves to change the current supplied by negative voltage pass transistor **19** in accordance with the current to be passed through load **14**. The voltage drop due to load current through current sensing resistor **11** is applied over line **24** and through input resistor **25** to inverting input terminal **26** of operational amplifier **23**. The non-inverting input **29** is connected across shunt resistor **30** and through input series resistor **28** and over line **27** to resistor terminal **71**. This input circuit to amplifier **23** is a differential input sensing only the drop across resistor **11** and unaffected by common mode voltage which may exist in the load lead between terminal **71** and the load ground terminal **13**. The current induced voltage drop across resistor **11** is amplified by amplifier **23** by a predetermined amount equal to the ratio of feedback resistor **31** to input resistor **25** and appears at output terminal **32** of amplifier **23**. This voltage is unidirectionalized (i.e. its absolute value is repeated) by a circuit comprising diodes **34** and **35** connected in opposition between junction point **33** and ground connected between output operational amplifier **36** has its non-inverting input **38** connected to the junction between diodes **34** and **35** over lead **37** and its inverting input **40** connected through input resistor **39** to junction point **33** and feedback resistor **41** connected between inverting input **40** and output terminal **42** of amplifier **36**. The gain of the amplifier is equal to **1** as determined by the ratio of feedback resistor **41** to input resistor **39**. When the voltage at the output terminal **32** is positive with respect to ground, diode **34** conducts, diode **35** is back biassed and the positive voltage at output terminal **32** is applied over line **37** to non-inverting input **38** to be amplified by the gain of amplifier **36** to appear at its output terminal **42** amplified and positive with respect to ground. When the output of amplifier **23** at terminal **32** is negative, diode **34** is back biassed and diode **35** conducts in effect grounding non-inverting input terminal **38** and thereby applying the output voltage of amplifier **23** to inverting input terminal **40** to be amplified and inverted by amplifier **36** to appear at output terminal **42** again as an amplified voltage positive with respect to ground. Thus, the output of amplifier **23** is amplified and unidirectionalized by the circuit just described. The unidirectionalized voltage is applied through resistor **43** at junction poine **56** to inverting input terminal **58** of amplifier **57**. This positive current at junction point **56** must be balanced by an equal negative current from the first feedback of the second control loop. This negative current is generated by the voltage at the output **53** of amplifier **47** through resistor **55** and is proportional to the drop across the current sensing resistors **18** and **10**. This voltage across resistors **18** and **10** will change until a balance is achieved between input terminals **58** and **59** of amplifier **57**. Thus, the second current control loop changes the current passed by negative polarity pass transistor **19** as a function of the load current demand and maintains the quiescent current in both pass devices.

Typical resistor values in this second current control loop are as follows (for a ±2 ampere power supply):

resistor **11**=0.25 ohm
resistor **28**=750 ohms
resistor **30**=15K ohms
resistor **25**=750 ohms
resistor **31**=15K ohms
resistor **39**=10K ohms
resistor **41**=10K ohms

The above description covers the operation of this bipolar regulator as a voltage programmed regulator. Similar operation is provided when the regulator is used as a current regulator. Basically the current regulating operation is provided by feeding back a load current sensed voltage rather than the load voltage. One way to accomplish current regulation is to apply the load current sensed and amplified voltage appearing at the output terminal **32** of amplifier **23** to the non-inverting input **3** of amplifier **4** over lead **70** by closing switch contacts **67–69** and opening switch contacts **67–68** and thereby comparing load current with the input signals from source **1** (rather than load voltage). Othewise the regulator operates as described above.

While the preferred form of the invention has been shown and described above, modifications are possible within the spirit and scope of the invention as set forth, in particular, in the appended claims.

I claim:

1. In a bipolar regulated power supply the combination of;

a pair of load terminals;

a first circuit connected across said load terminals including, in series a source of voltage of one polarity, a first signal controllable pass device, a first current sensing resistor and a second current sensing resistor;

a second circuit connected across said load terminals including in series, a source of voltage of a second polarity, a second signal controllable pass device, a third current sensing resistor having a value equal to said first current sensing resistor and said second current sensing resistor;

means for controlling said first signal controllable pass device including a source of input signals and a load voltage or current feedback circuit;

and means for maintaining a substantially constant quiescent current through both of said pass devices in addition to bipolar current to said load terminals if any;

wherein said means for maintaining a substantially constant quiescent current includes two interdependent control circuits coupled to control said second pass device, one including means for sensing the voltage across said first and third current sensing resistors taken in series and the second including means for sensing the voltage across said second current sensing resistor;

means for repeating the absolute value of the latter said voltage;

and means for combining said first said sensed voltage and said repeated voltage to provide said control to said second pass device.

2. A bipolar regulated power supply as set forth in claim **1**, and;

wherein said source of input signals is for controlling the voltage across the load terminals;

and said feedback circuit is derived from means for sensing voltage across said load terminals.

3. A bipolar regulated power supply as set forth in claim **1**, and;

wherein said source of input signals is for controlling the current to said load terminals;

and said feedback circuit is derived from means for sensing current to said load terminals.

* * * * *

United States Patent [19]

Nercessian

[11] **4,004,155**

[45] **Jan. 18, 1977**

[54] **BIPOLAR REGULATED HIGH VOLTAGE POWER SUPPLY**

[75] Inventor: **Sarkis Nercessian,** Flushing, N.Y.

[73] Assignee: **Forbro Design Corporation,** New York, N.Y.

[22] Filed: **Oct. 3, 1975**

[21] Appl. No.: **619,444**

[52] **U.S. Cl.** **307/52;** 307/72

[51] **Int. Cl.²** **H02J 3/38**

[58] **Field of Search** 307/52, 72, 75, 43, 307/51, 44

[56] **References Cited**

UNITED STATES PATENTS

2,772,387 11/1956 Liguori ..... 307/72 X

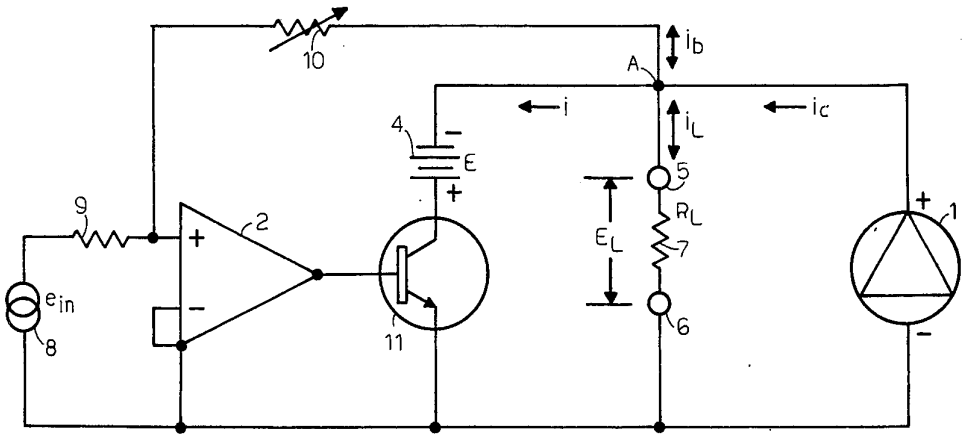
Primary Examiner—Herman J. Hohauser

Attorney, Agent, or Firm—Alfred W. Barber

[57] **ABSTRACT**

Two sources of current are applied to a load. One source supplies a constant current which is at least equal to the maximum current to be supplied to the load in one polarity. The second source is in opposition to the first source and is capable of being controlled from zero to a value at least double the value of the constant current. A voltage feedback circuit in combination with a bipolar control signal provides a bipolar voltage across the load having maximum positive and negative voltage excursions equal to the control signal times the feedback circuit gain and current in either direction having a maximum value substantially equal to the constant current value. In this manner a high voltage regulated bipolar voltage can be controlled across a load using one controlled unipolar device while providing class A operation, that is, without cross-over distortion. An important feature of the invention is the positive and negative limiting of both load voltage and load current.

5 Claims, 6 Drawing Figures



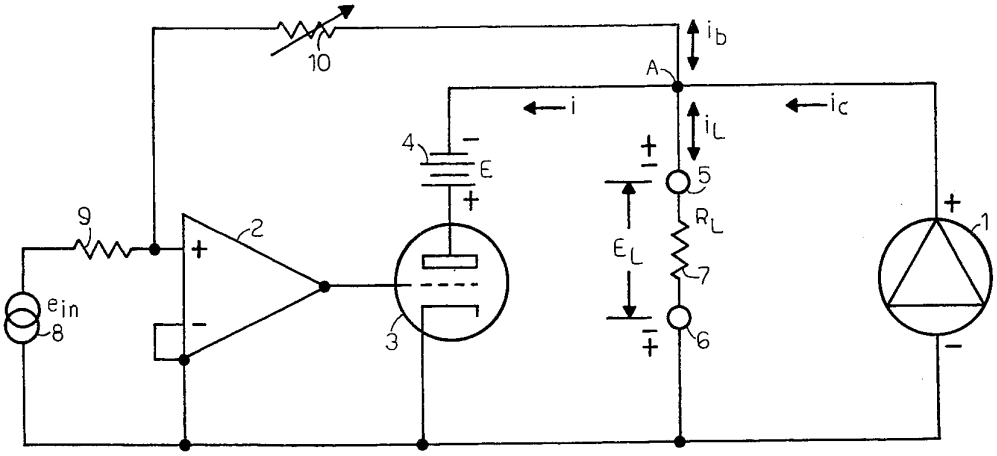

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FIG. 1

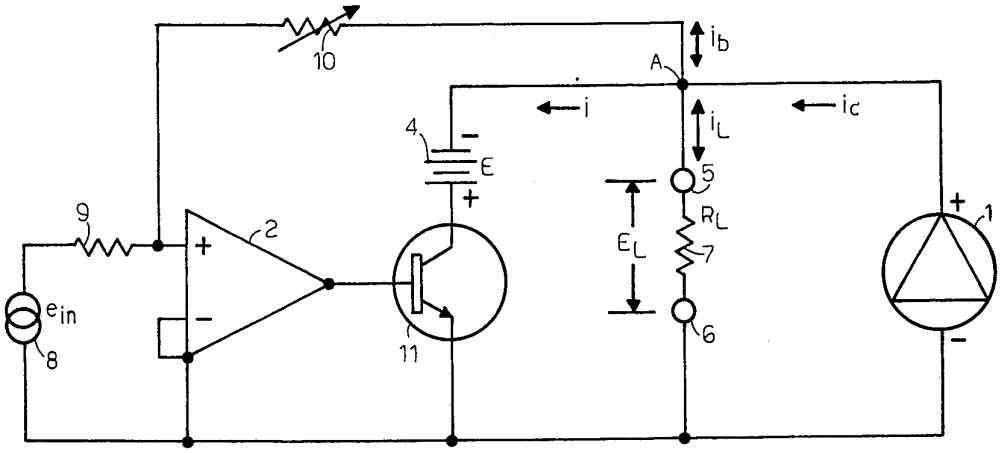
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FIG. 2

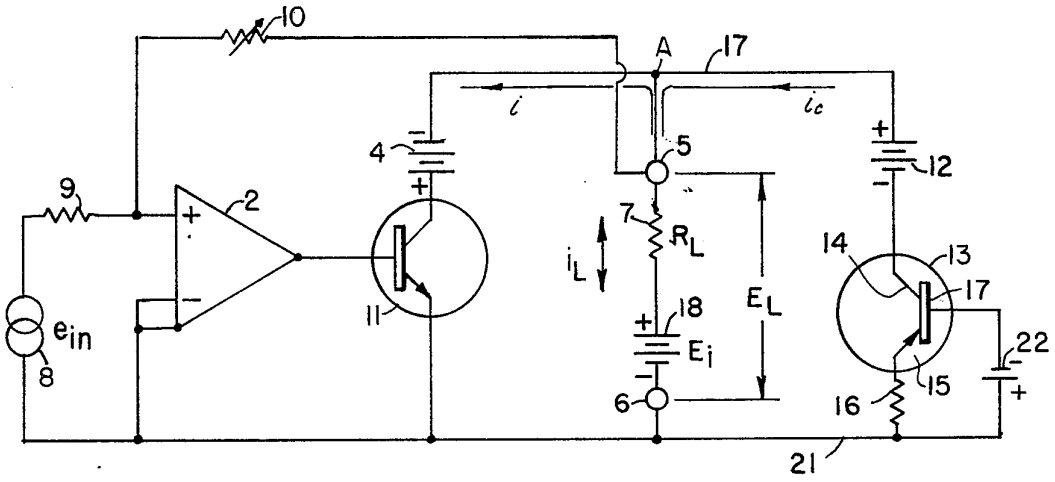
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FIG. 3

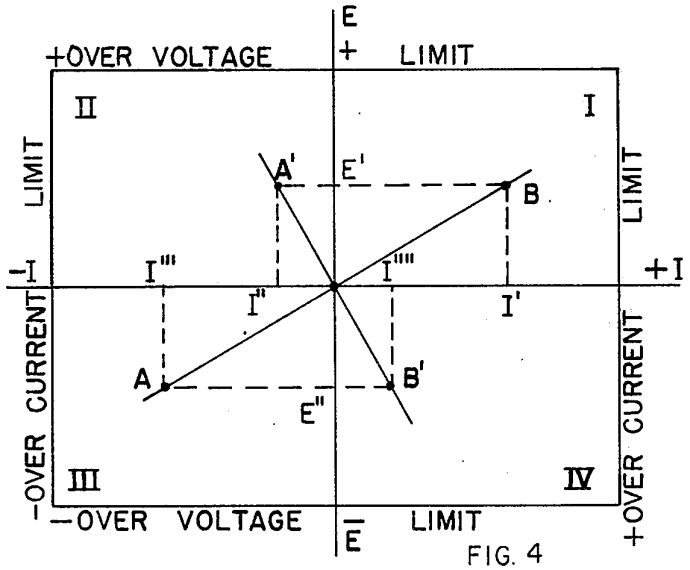

E
+OVER VOLTAGE
+ LIMIT
II
I
LIMIT
LIMIT
A'
E'
B
-I
I'''
I''''
+I
I''
I'
A
B'
E''
-OVER CURRENT
+OVER CURRENT
III
IV
-OVER VOLTAGE
- LIMIT
E

FIG. 4

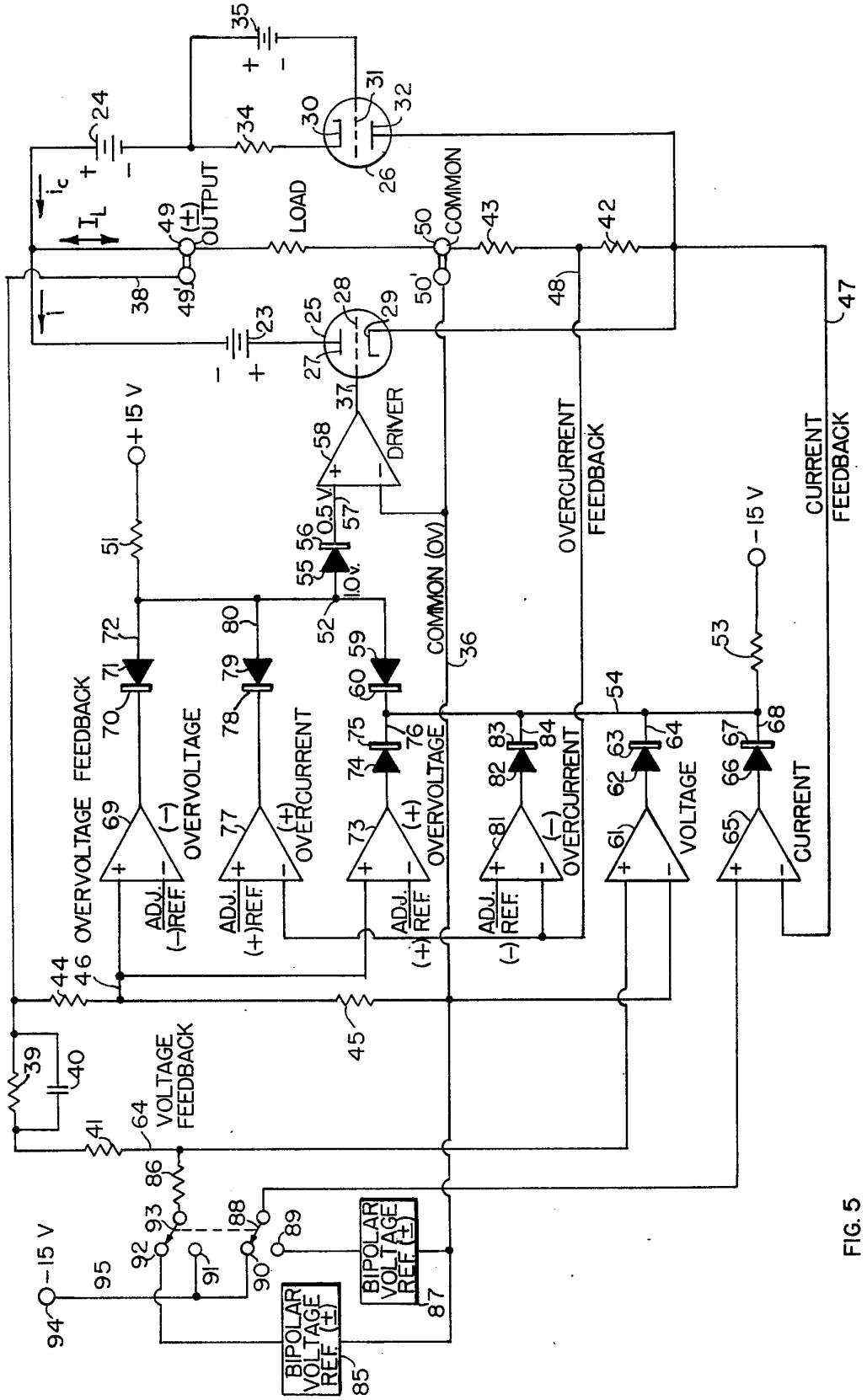
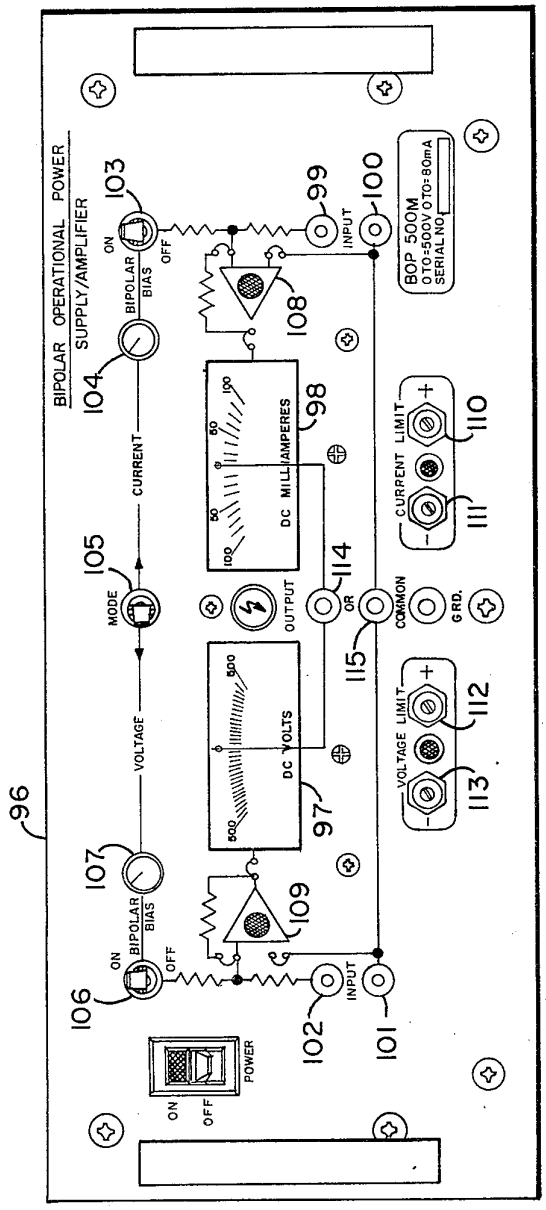

+15 V
-15 V
OUTPUT
LOAD
COMMON
DRIVER
0.5 V
10 V
COMMON (OV)
OVERCURRENT FEEDBACK
CURRENT FEEDBACK
OVERVOLTAGE FEEDBACK
VOLTAGE FEEDBACK
OVERVOLTAGE
OVERCURRENT
VOLTAGE
CURRENT
ADJ. REF.
BIPOLAR VOLTAGE REF (±)

FIG. 5


BIPOLAR OPERATIONAL POWER SUPPLY/AMPLIFIER
BOP 500M
0 TO ±500V 0 TO ±80mA
SERIAL NO.
ON
OFF
BIPOLAR BIAS
INPUT
CURRENT
VOLTAGE
MODE
OUTPUT
DC MILLIAMPERES
DC VOLTS
CURRENT LIMIT
VOLTAGE LIMIT
COMMON
GRD.
POWER
96
97
98
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111
112
113
114
115

FIG. 6

BIPOLAR REGULATED HIGH VOLTAGE POWER SUPPLY

PRIOR ART

In the past, class A bipolar operation has been provided using vacuum tubes or transistors and phase inverting transformers. Such circuits could not respond to direct current and so were quite unsuited to power supply use. When complementary transistors (PNP and NPN) became available, complementary symmetry bipolar circuits responding to direct current were possible. One example of the latter in a power supply configuration is shown and described in U.S. Pat. No. 3,566,292. The circuitry is complicated by the necessity for driving two output control devices, one in one direction and the other in the other direction. Furthermore, positive and negative limiting of the output voltage or current has been awkward and not easily adjusted or programmed.

SUMMARY

It has been found possible to provide a well regulated, cross-over distortion free bipolar output using a source of constant current in conjunction with one programmed unipolar device. The source of constant current must supply the maximum load current in one polarity and have a compliance range equal to the maximum required output voltage. The source of constant current need not be well regulated since the essential regulation and control is provided by the second source of current. The second source of current is feedback regulated from the load voltage or current and must supply at least twice the maximum load current at the maximum load voltage or current. The second source receives a bipolar input programming voltage and the feedback circuit sets the voltage gain to the load.

In operation, the constant current source supplies a constant current to the load at the maximum rated load voltage. If the second source is cut off, the load voltage and current are maximum in the polarity direction of the constant current source. In order to control the load voltage, a programmable second source of current poled oppositely to the constant current source is also connnected across the load. It can now be seen that if the second source is cut off, the load voltage and current will be maximum in one polarity; if the current from the second source equals the constant current, the load voltage and current will be zero; and if the current from the second source is twice the constant current, the load voltage and current will be maximum with a polarity opposite to that of the polarity of the first current source. Thus, by controlling the second source with a bipolar input voltage, the load voltage will be programmed bipolar from maximum in one polarity to maximum in the opposite polarity. Since there is no discontinuity at cross-over, the system operates class A showing no cross-over distortion.

In the drawing:

FIG. 1 is a simplified circuit diagram of the basic form of the present invention.

FIG. 2 is a simplified circuit diagram of the form of FIG. 1 employing a transistor rather than vacuum tube for controlling the load voltage.

FIG. 3 is similar to FIG. 2 except details of one form of constant current source are shown.

FIG. 4 is a graphical representation of four quadrant operation of the circuit of the invention.

FIG. 5 is a simplified circuit diagram of the preferred form of the invention.

FIG. 6 shows one form of front panel layout suitable for the invention.

FIG. 1 is a circuit in which a source of constant current 1 and a unipolar voltage regulating circuit including control amplifier 2, pass the tube 3 and unregulated voltage source 4, are connected in parallel across a pair of load terminals 5 and 6. A load such as resistor 7 to be supplied with regulated voltage is connected between load terminals 5 and 6. The voltage regulating circuit is completed by a source of input or programming voltage 8, a reference or input resistor 9 and a feedback or gain control resistor 10. The input voltage 8 is symbolically represented as an alternating current voltage since the system is intended to accept a bipolar input or control voltage and to deliver to the load terminals and load a regulated bipolar voltage. The load voltage will be:

$$E_L = e_{in}\frac{R_{10}}{R_9} \qquad \begin{matrix} R_{10} = \text{resistance of 10} \\ R_9 = \text{resistance of 9} \end{matrix}$$

as in the familiar bridge regulated power supply. The bipolar capability is provided by the use of the constant current source.

Considering the currents entering and leaving junction point A, constant current source 1 provides a constant current i_c, pass tube 3 draws a regulating current i, a small bridge current i_b flows through resistor 10 and a load current i_L flows through load resistance R_L. Neglecting i_b the load current is $i_1 = i_c - i$. It will be seen that if i is less than i_c, the current will flow downward through load R_L and terminal 5 will be positive with respect to terminal 6 while if i is greater than i_c, the current flow and polarity will be reversed. Thus, by controlling i from 0 to $2i_c$ the load can be controlled from a current equal to i_c in one direction to $-i_c$ in the opposite direction. The load voltage can be controlled to be bipolar by controlling the unipolar current i in the presence of a constant current i_c also unipolar.

The above seems to imply that load current i_L is necessary in programming load voltage. Actually load voltage may be controlled in the absence of load current (R_L infinite) due to the presence of the bridge current i_b which, in fact, determines the load voltage and its polarity. In such case the constant current i_c flows through regulating elements 3 and 4. It should be noted that when $i = i_c$, the load current (and hence voltage) is zero but since there is no discontinuity at this point, there is no cross-over distortion. In other words, two unipolar control devices are capable of providing a regulated bipolar voltage at a load without cross-over distortion.

FIG. 2 is similar to FIG. 1 and operates in the same way except the unidirectional control device is transistor 11 instead of the vacuum tube 3. The operation is otherwise the same as described above in connection with FIG. 1 and the same numerals are used to designate corresponding components of the circuit.

FIG. 3 is similar to FIG. 2 but with the addition of details of one form of constant current circuit which may be employed as the constant current source 1. The constant current source comprises a source of dc voltage represented by battery 12 with the positive termi-

nal connected to load terminal **5.** A transistor **13** including a collector **14,** an emitter **15** and a base **17** is connected with collector **14** connected to the negative terminal of voltage source **12,** emitter **15** connected through a fixed resistor **16** to load terminal **6** over lead **21,** and base **17** connected to a source of reference voltage **22.** The constant current provided by this circuit is approximately equal to the voltage across battery **22** divided by the resistance of resistor **16.** The constant current so provided (*ic*) will be maintained as long as the voltage source as represented by battery **12** is sufficient to sustain the load voltage called for by the control circuit (**2-4-8-9-10-11**). As explained above, this is a bipolar circuit providing current through the load in either direction all controlled by a unipolar control circuit.

FIG. **3** illustrates one further point with respect to the operation of the invention. This is operation with an active load. A passive load would be one such as resistor **7** connected *b* between load terminals **5** and **6.** Such a load will provide two quadrant operation of the E, I output domain, more fully explained below. However, the addition of a source of voltage such as that represented by battery **18** in series with the load resistor provides what may be termed an "active load" and may cause the power supply to operate in two additional quadrants of the E, I domain.

FIG. **4** taken with FIG. **3** may be used to explain passive and active load operation, Let E′ be a positive voltage programmed across load terminals **5–6** and E″ a negative voltage also programmed across the load terminals. With E_1 absent or zero the positive voltage E′ will cause a current I′ to flow in load resistor **7** (R_L) found by the intersection of voltage line E′ with load line AB. Similarly, the negative voltage E″ will cause a negative current I″ to flow through the load resistor as determined by the intersection of the E″ voltage line with the load line AB at A. This defines operation in quadrant I and III.

An active load, as stated above, is one having a voltage in series with the load such at that represented by battery **18** in FIG. **3.** Now if active voltage E_1 is greater than E′ or E″, the direction of current will be reversed becoming negative (I″) for E′ and positive (I″″) for the negative voltage E″ as defined by points A′ and B′ on load line A′B′. This operation takes place in quadrants II and IV respectively.

It has been found that the above described four quadrant operation requires novel operating restraints. First, voltage and current limiting must be supplied in four quadrants i.e. positive voltage limiting, negative voltage limiting, positive current limiting and negative current limiting. Second, it has been found in a system such as the one being described that if one applied simultaneous bipolar voltage and bipolar current programming, undesirable or impractical conditions can develop. Accordingly, an important feature of the present invention is the provision for selecting, exclusively, voltage or corrent bipolar programming while maintaining positive and negative current and voltage limiting. Furthermore, the current and voltage limits are all independently settable providing limiting in all four quadrants of operation. Characteristic upper and lower voltage and current limit lines are shown on FIG. **4.** How they are implemented is described below.

The following general remarks provide a background for the specifics of FIG. **5.** In the voltage mode of operation, the voltage feedback is taken from the load in such a manner that the control tube **25** introduces a 180° phase inversion. On the other hand, the current mode operation uses a feedback from resistors connected in the cathode circuit of the control tube and there is no phase inversion due to the control tube. Since the power supply in either mode must operate with overall degenerative feedback (total 180° phase shift) the amplifiers preceeding the gates and operating on the voltage mode amplifier have feedback returned to non-inverting inputs while the amplifiers operating on current mode have feedback returned to inverting inputs.

Assuming for the sake of explanation of the circuit operation that a predetermined point at the junction of all control gates is to be maintained at a predetermined potential, say plus 1 volt, the various gates must be connected so that they tend to hold this point down to 1 volt or in the case of over voltage or over current conditions to tend to reduce the potential below the 1 volt normal level. One way to accomplish the above is to provide a positive and negative source of voltage connected through two current limiting resistors, the positive source connected to the predetermined point directly through its resistor and the negative source connected through its resistor and a diode poled to conduct from the positive source to the negative source. Some of the diode gates are connected to one side of this latter diode and some to the other side as described below in connection with FIG. **5.**

FIG. **5** shows how various feedback voltages are derived in order to provide voltage programming, current programming, over-voltage control and over-current control. A control tube **25** including a plate **27,** grid **28** and cathode **29** (heated by suitable means, not shown) is controlled over line **37** connected to grid **28** and receives plate voltage from a suitable source represented by battery **23.** The constant current is supplied by a second vaccum tube **26** including a plate **32,** a grid **31** and a cathode **30** (heated by suitable means, not shown). A suitable supply voltage is provided by a suitable source represented by battery **24.** Constant current is determined by means of grid bias battery **35** and cathode resistor **34** as described above. The bipolar output from this two tube circuit is applied to output terminals **49** and **50.** Voltage sensing terminals **49′** and **50′** are used for control circuit connections. This circuit is particularly intended for a high voltage, bipolar power supply with independent output voltage and current control and maximum current and voltage limiting in all four quadrants of the operating E, I domain (see FIG. **4**). In order to provide for current control and overcurrent limiting two current sensing resistors, **42** and **43,** are connected in series in the output line going to common output sensing terminal **50′**. The over-current sensing is taken across resistor **43** over line **48** while the current control sensing is taken across both resistors **42** and **43** in series over line **47.** The voltage feedback circuits are also referenced to output sensing terminal **50′** and comprises two circuits branched from lead **38** taken from load voltage sensing terminal **49′**; one, the voltage control line **64** being taken through resistor **39** shunted by lag capacitor **40** in series with resistor **41;** and the other, the over-voltage line **46** taken at the junction between attenuator resistors **44** and **45.**

FIG. **5** also contains a simplified schematic showing the amplifiers and gates used to provide the operative four quadrant control and limiting circuits. A driver

amplifier 58 provides a control output over line 37 to grid 28 of control tube 25. In order to understand the operation of the important features of the invention it is assumed that amplifier 58 has a very high gain so that at its input line 57 the control voltage is always very close to a characteristic voltage, say 0.5 volt. In the discussion that follows, for the sake of clarity of the explanation it will be assumed that all diodes (used as gates) have a forward drop of 0.5 volt. Thus, the operating potential at junction point 52 will be 1.0 volt.

Junction point 52 receives a current from a positive source of voltage (+ 15v) through current limiting resistor 51. Three gate diodes 59–60, 70–71 and 78–79 are connected with their respective anodes 59, 71 and 79 directed to junction point 52. The gate diode seeing the least positive potential will control the potential of junction point 52 since any gate seeing a higher potential will block this potential due to its cathode to anode direction of connection. Consider the over-voltage (negative) limiting. The sensed voltage over lead 46 is applied to the non-inverting input of amplifier 69 while a negative reference voltage is applied to its inverting input. As long as the output voltage is greater than the reference (less negative) the output of amplifier 69 will be positive generally sitting at its positive output saturation voltage. However, if the output voltage approaches a negative limit as determined by the setting of a negative reference, the output of amplifier 69 will start to fall and when it reaches a point which is less positive than 0.5 volt this gated voltage through gate diode 70–71 will assume control preventing the output of the power supply from going any further negative by controlling amplifier 58 through its input diode 55–56.

The over current control is provided by amplifier 77 operating through gate diode 78–79 to junction point 52. The overcurrent sensing lead 48 is connected to the inverting input of amplifier 77 and an adjustable positive reference is connected to the non-inverting input. This provides the positive over-current limit since the polarity of the current feedback is opposite to that of the over-voltage feedback. When the current approaches the preset reference positively the output of amplifier 77 starts to drop and takes control when the output starts to drop below 0.5 volt.

In order to provide the required control from the other control means, namely, the output voltage control, the output current control, positive over-voltage and negative over-current, a control line 54 is connected through diode gate 59–60 to junction point 52, and all of the controls just named are gated anode to cathode to this line and a source of negative bias current is applied to it from a negative voltage source (−15v.) through current limiting resistor 53. control by the feedback circuits connected to line 54 is exerted by the least negative (more positive) voltage coupled through one of the anode to cathode gate diodes. The control will be exerted by the circuit providing plus 1 volt through its gate to line 54 which in turn will sit at 0.5 volt and through gate diode 59–60 will control junction point 52 at plus 1 volt.

Four feedback circuits are gated to line 54. The output voltage control feedback line 64 is connected to the non-inverting input of comparison amplifier 61 while the bipolar control voltage from source 85 connected through resistor 86 is applied to the non-inverting input and the output is coupled to line 54 through the anode 62 to cathode 63 gate diode. The output current control feedback over line 47, being of opposite polarity, is applied to the inverting input of amplifier 65, a bipolar control voltage from source 87 is connected to the non-inverting input through switch 88–89 when switched to current control position and the output is coupled through the anode 66 to cathode 67 gate diode, over line 68 to line 54. The voltage limit feedback over line 46 is applied to the non-inverting input of amplifier 73; an adjustable positive limit reference voltage is applied to the inverting input and the output is coupled through anode 74 to cathode 75 gate diode over line 76 to line 54. The current limit feedback line 48 is applied to the inverting input of amplifier 81, an adjustable negative limit reference is applied to the non-inverting input and the output is coupled through anode 82 to cathode 83 gate diode over line 84 to line 54. All of the above mentioned polarities are with respect to common sensing terminal 50'.

As mentioned above, undesirable or impractical conditions can develop in a bipolar power supply subjected to simultaneous voltage and current control. Accordingly, means are provided to select voltage or current control or programming each to the exclusion of the other. Means for doing this is double-pole double-throw switch 88–89–90–91–92–93. With switch arms 88 and 93 in their upper positions, as shown, voltage control of the power supply is provided since arm 93 closing to contact 92 closes the circuit from bipolar voltage control source 85 through input resistor 86 to the non-inverting input of voltage control amplifier 61 thereby providing bipolar voltage control of the power supply. At the same time switch arm 88 closed to contact 90 places negative 15 volts at terminal 94 over lead 95 to the non-inverting input of current amplifier 65 thereby cutting off current control of the power supply leaving the voltage programming or control unaffected by the current control circuit. In a similar manner, exclusive current control or programming is provided by moving switch arms 88 and 93 to their lower positions. When this is done, the bipolar current programming source 87 is connected through contact 89 and switch arm 88 to the non-inverting input of current control amplifier 65 thereby providing bipolar current programming of the power supply. At the same time any possible effect of the voltage control through amplifier 61 is removed by the negative bias on terminal 94 applied over lead 95, through switch contact 91 to arm 95 and through resistor 86 to the non-inverting input of amplifier 61. In this way voltage control is cut-off so that the bipolar current programming is in exclusive control. However, the voltage limit (+ and −) and the current limit (+ and −) amplifiers will exert overriding influences should either the voltage or current requested at output terminals 49–50 exceed the preset limits on the limit controls.

Restating the general operation of the bipolar power supply described above, the power supply output is exclusively programmed or controlled in either bipolar voltage mode or bipolar current mode while at the same time adjustable positive and negative voltage and current limits are provided. The diode gating as described above insures this overall operation.

FIG. 6 shows one form of front panel layout suitable for the invention described above. Front panel 96 carries a center-reading voltmeter 97 for observing the direct current component of the output voltage and a center-reading current meter 98 for observing the direct current component of the output current. Input terminals for current programming 99 and 100 and

input terminals for voltage programming **101** and **102** are provided. Switch **103** when in its up position (ON), connects an internal bipolar reference for current control through bias control potentiometer **104** to mode selector switch **105** while switch **106** when in its up position, connects a bipolar reference for voltage control through bias control potentiometer **107** to mode selector switch **105.** Mode selector switch **105** selects either current or voltage control (corresponding to switch **88** through **93** in FIG. **5**). The current mode amplifier is shown diagrammed as **108** and the voltage mode amplifier as **109.** The adjustable current limit controls are **110** for positive limit and **111** for negative limit. The voltage limit controls are **112** for positive limit and **113** for negative limit. The output binding posts are at **114** and **115.** The various lines and resistors shown on the panel are to illustrate the actual internal connections. Thus, the front panel shows the basic organization of the power supply controls and terminals as an assist in using same.

While the preferred form of the invention shown in FIG. **5** employs vacuum tubes for current source and control, transistors may also be used. Other modifications are anticipated which fall within the scope of the invention as set forth in particular in the appended claims.

I claim:

1. In a bipolar regulated power supply, the combination of;

a pair of load terminals;

a source of first DC current of a first polarity connected through a current sensing resistor and across said load terminals;

a source of a second DC current of a polarity opposite to said first polarity connected to said load terminals through said current sensing resistor;

current control means connected in series with said source of said second current capable of controlling said second current from a value equal to a small fraction of the value of said first current to a value substantially twice the value of said first current whereby bipolar voltage or current is provided to said terminals;

wherein said control means includes; a voltage control amplifier for receiving a sample of the terminal voltage and comparing it with a first bipolar reference for controlling the voltage across said terminals in accordance with said comparison; a current control amplifier for receiving a sample of the terminal current and comparing it with a second bipolar reference for controlling the current to said terminals in accordance with said comparison; adjustable positive overvoltage control means; adjustable negative overvoltage control means; adjustable positive overcurrent control means; adjustable negative overcurrent control means;

and means for exclusively selecting control by said voltage control amplifier or said current control amplifier while retaining all four overvoltage or overcurrent control means.

2. A bipolar regulated power supply as set forth in claim **1,** and wherein;

said adjustable overvoltage and overcurrent control means include independently adjustable references and amplifiers for comparing feedback voltages and currents with said references;

whereby each of the four overvoltage and overcurrent limits can be set independently.

3. A bipolar regulated power supply as set forth in claim **1,** and wherein;

each of said control means includes a comparison amplifier for comparing a reference voltage with a feedback voltage and output gating means from said amplifiers to said current control means whereby one of said amplifiers is in exclusive control of the voltage or current to said load terminals.

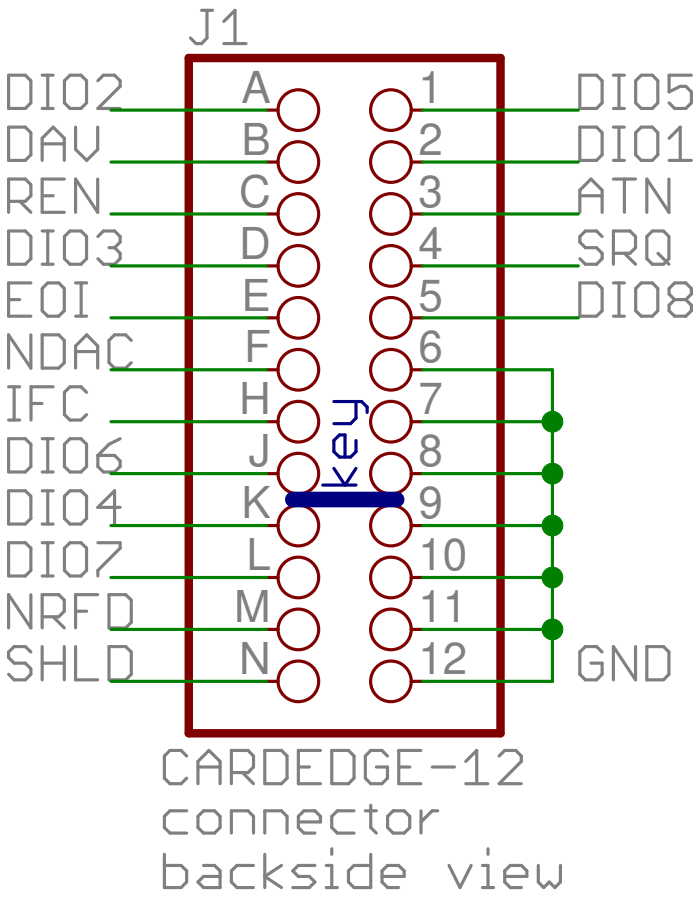
4. A bipolar regulated power supply as set forth in claim **1,** and wherein;

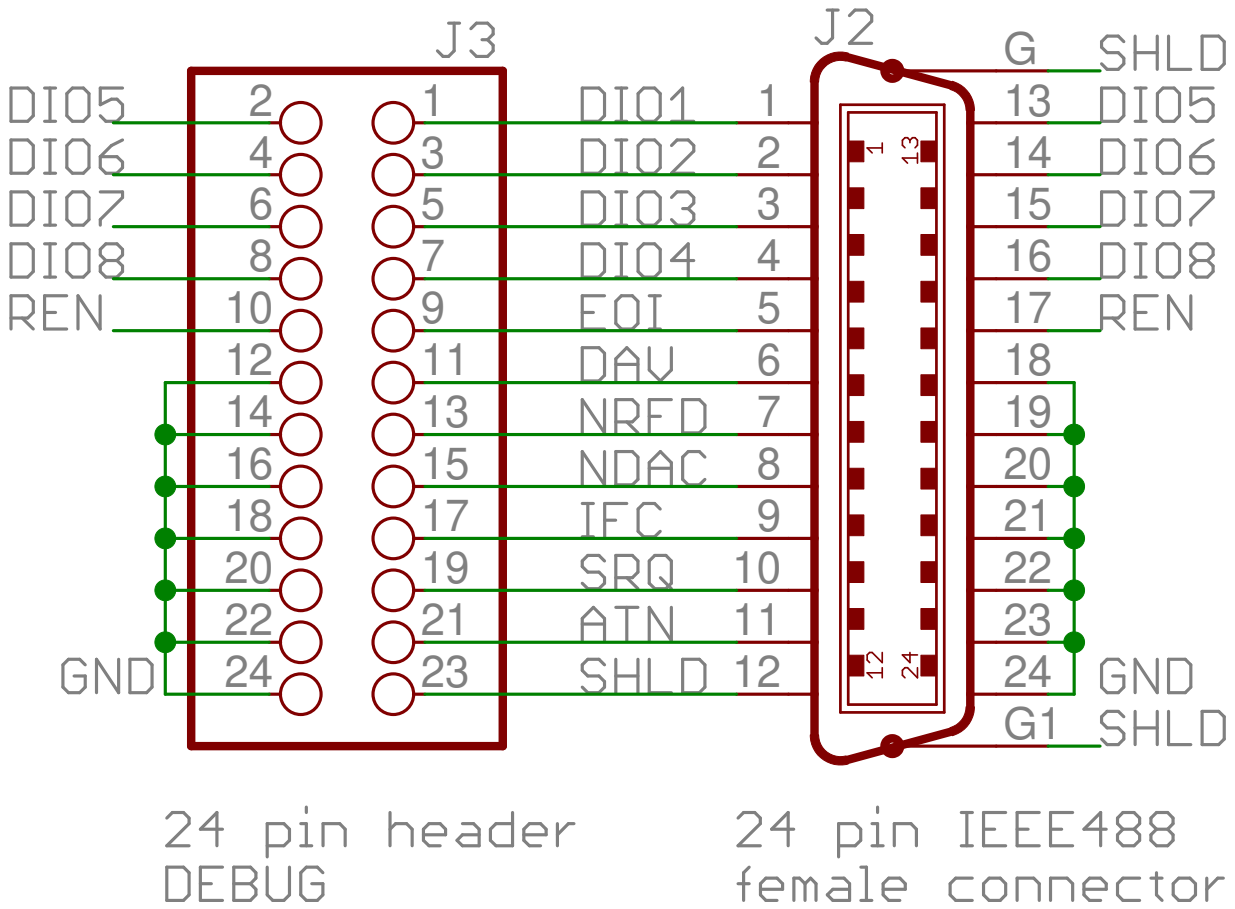
said current control means includes at least one vacuum tube.

5. A bipolar regulated power supply as set forth in claim **1,** and wherein;

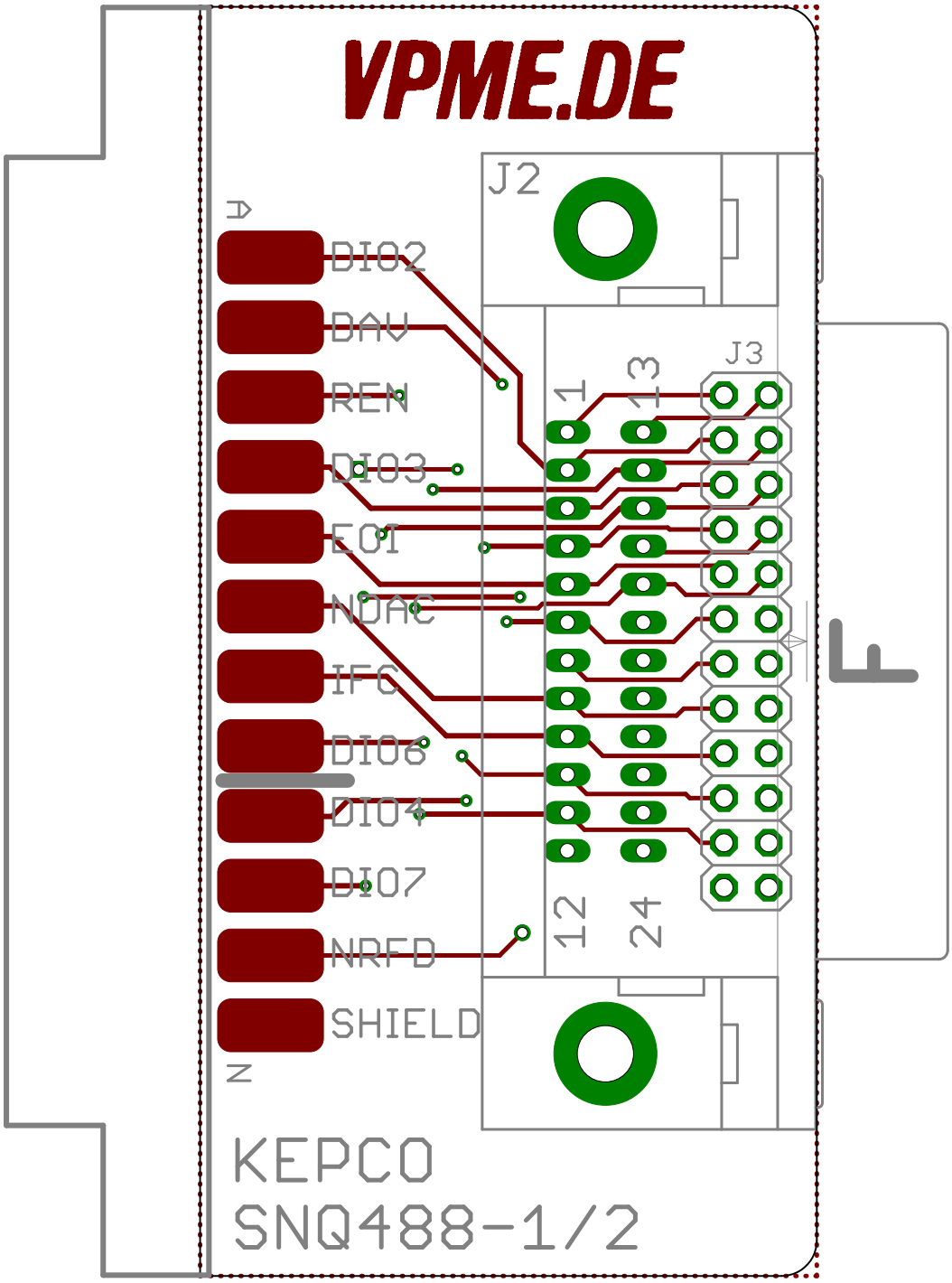
said adjustable control means provide voltage or current limiting from substantially zero voltage or current to the maximum safe limits of positive or negative voltage or current for the power supply.

* * * * *





KEPCO SNQ488-1/2 GPIB adapter


VPME.DE
J2
J3
1
13
12
24
DIO2
DAV
REN
DIO3
EOI
NDAC
IFC
DIO6
DIO4
DIO7
NRFD
SHIELD
KEPCO
SNQ488-1/2

United States Patent [19]

Nercessian

[11] **4,335,445**

[45] **Jun. 15, 1982**

[54] SYSTEM FOR INTERFACING COMPUTERS WITH PROGRAMMABLE POWER SUPPLIES

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[73] Assignee: **Kepco, Inc.**, Flushing, N.Y.

[21] Appl. No.: **15,453**

[22] Filed: **Feb. 26, 1979**

[51] **Int. Cl.**[3] **G06F 3/00**

[52] **U.S. Cl.** ..... **364/900**; 363/78; 340/347 M; 364/483

[58] **Field of Search** ..... 363/78, 79; 323/17, 323/322; 364/900 MS File, 200 MS File, 483; 340/347 DA, 347 SH, 347 M; 235/92 SH; 307/221 R; 330/297

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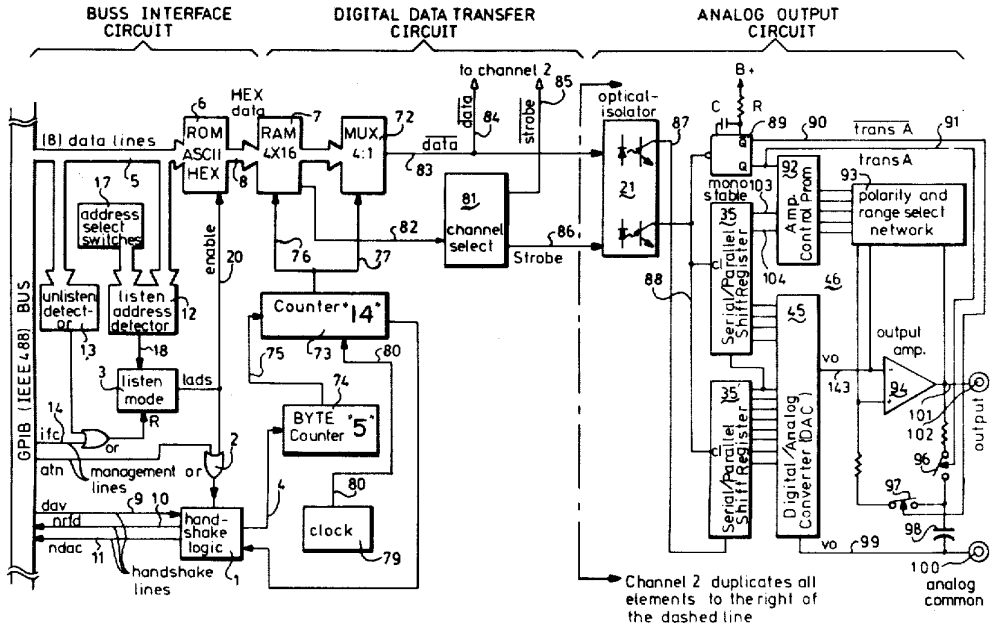
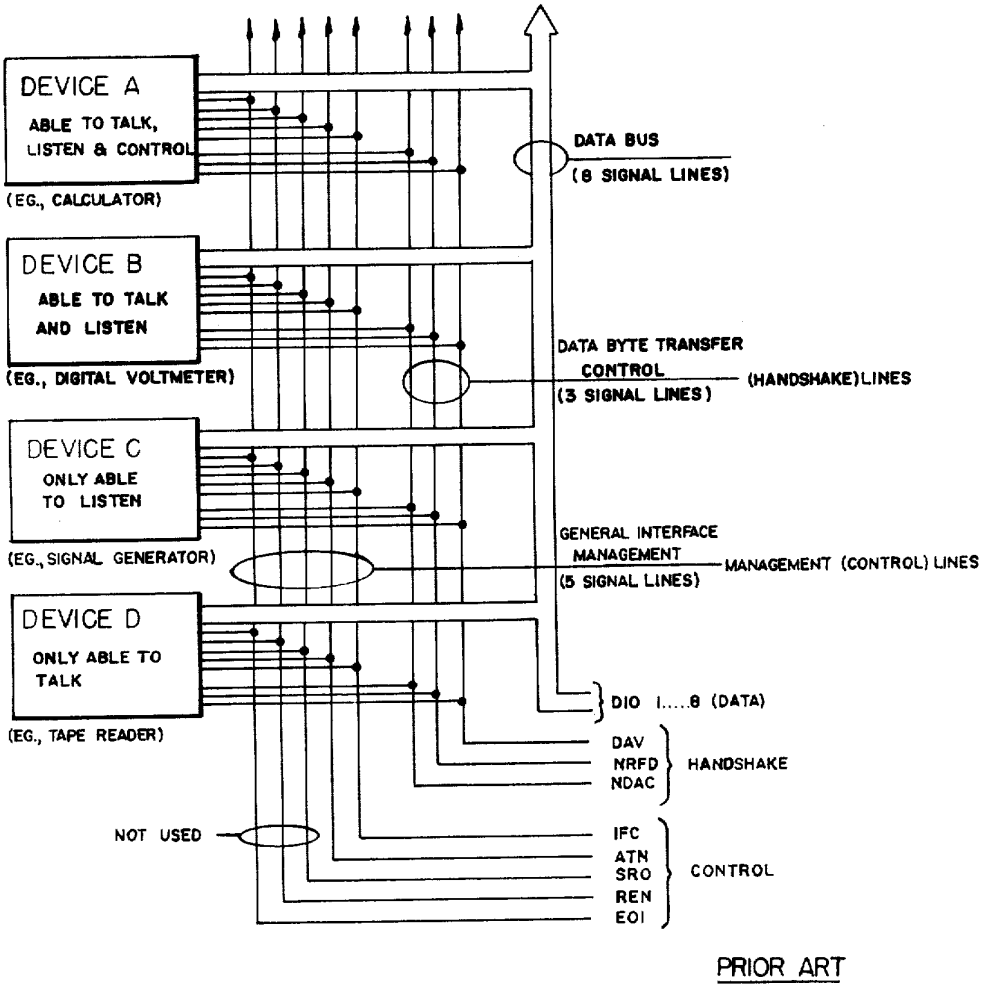
Primary Examiner—Gareth D. Shaw
Assistant Examiner—Eddie P. Chan
Attorney, Agent, or Firm—Alfred W. Barber

[57] **ABSTRACT**

Programmable power supplies as used in automatic testing systems (ATS) require three commands from a computer; namely, polarity, gain and analog magnitude. Whether received from a general purpose bus such as the IEEE 488 or other means the commands are in parallel format and must be serialized. The three commands must be recognized and decoded and applied to the appropriate power supplies. The present invention in addition to furnishing the above responses, provides optical isolation to eliminate possible ground loops and other voltage difference problems. One significant simplification comprises the use of sample and hold amplifiers in place of the more conventional latches so that new commands can be accumulated without affecting the response to a prior command.

3 Claims, 11 Drawing Figures





PRIOR ART

FIG. 1

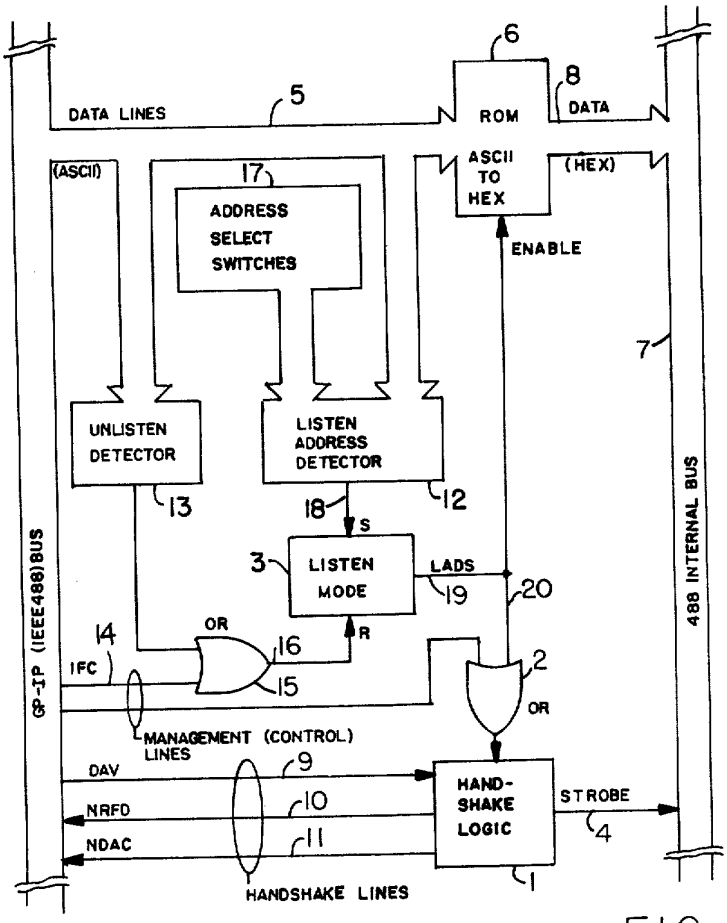

DATA LINES
5
6
ROM
8
DATA
(ASCII)
17
ADDRESS SELECT SWITCHES
ASCII TO HEX
(HEX)
ENABLE
7
UNLISTEN DETECTOR
13
LISTEN ADDRESS DETECTOR
12
18
S
3
LISTEN MODE
LADS
19
20
R
14
OR
16
IFC
15
2
OR
GP-IB (IEEE488) BUS
488 INTERNAL BUS
MANAGEMENT (CONTROL) LINES
DAV
9
NRFD
10
NDAC
11
HAND-SHAKE LOGIC
STROBE
4
1
HANDSHAKE LINES

FIG. 2

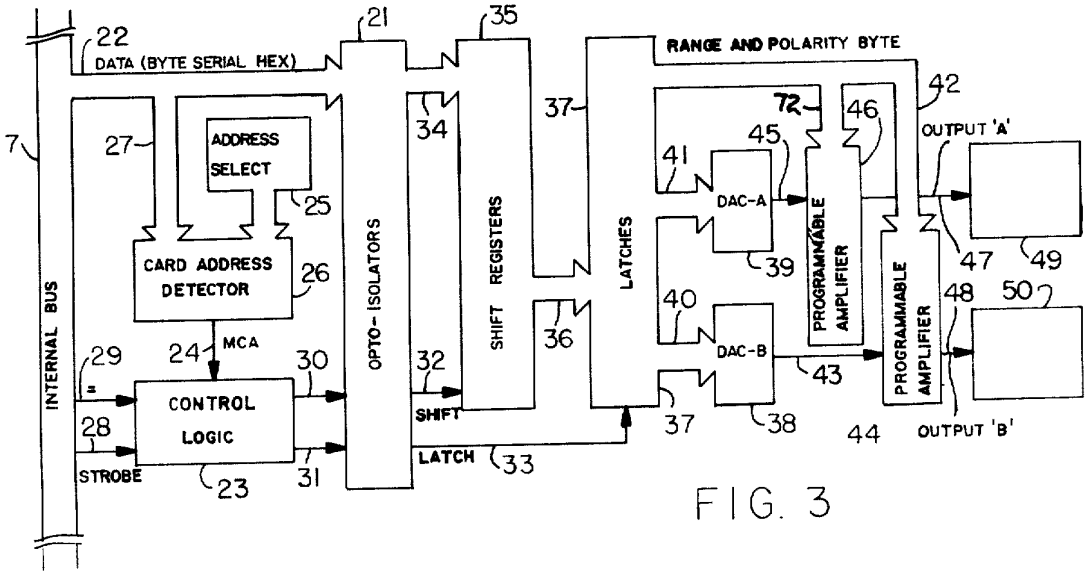

22
DATA (BYTE SERIAL HEX)
21
35
RANGE AND POLARITY BYTE
42
7
27
ADDRESS SELECT
25
CARD ADDRESS DETECTOR
26
24
MCA
29
30
28
CONTROL LOGIC
STROBE
23
31
INTERNAL BUS
OPTO-ISOLATORS
34
32
SHIFT
LATCH
33
SHIFT REGISTERS
36
37
LATCHES
72
46
45
41
DAC-A
39
40
DAC-B
38
43
PROGRAMMABLE AMPLIFIER
PROGRAMMABLE AMPLIFIER
48
50
47
49
OUTPUT 'A'
OUTPUT 'B'
44

FIG. 3

FIG.4

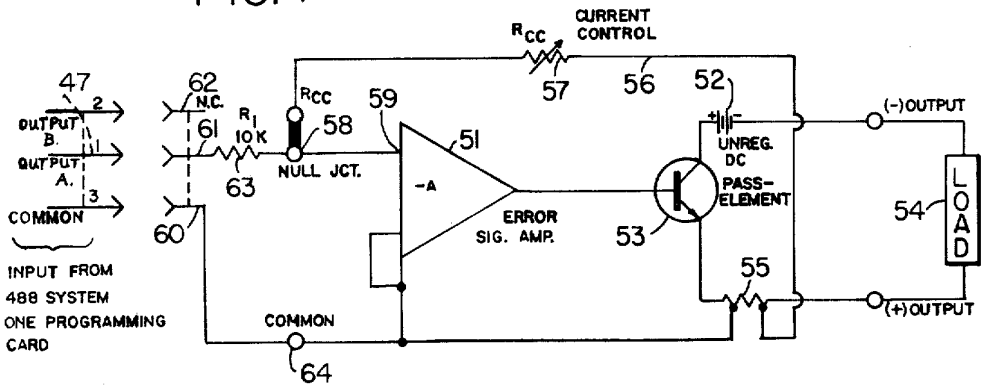


FIG.5

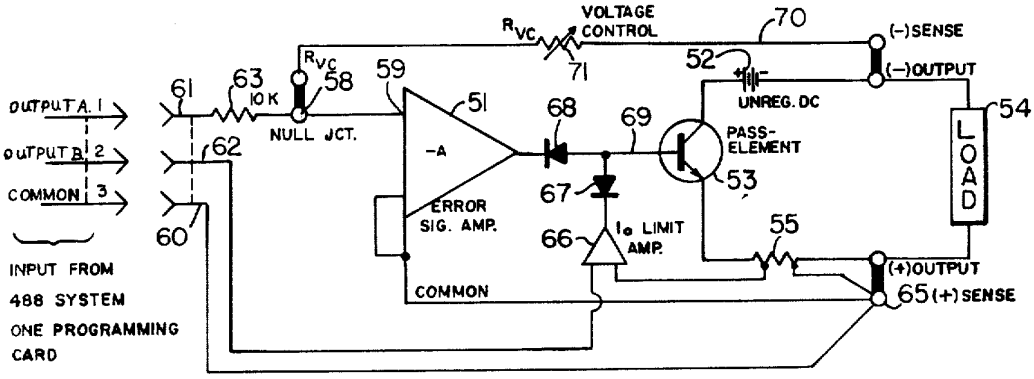
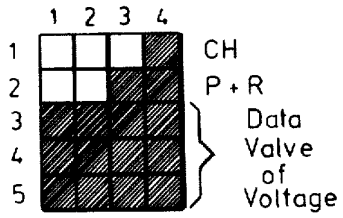


FIG.6A



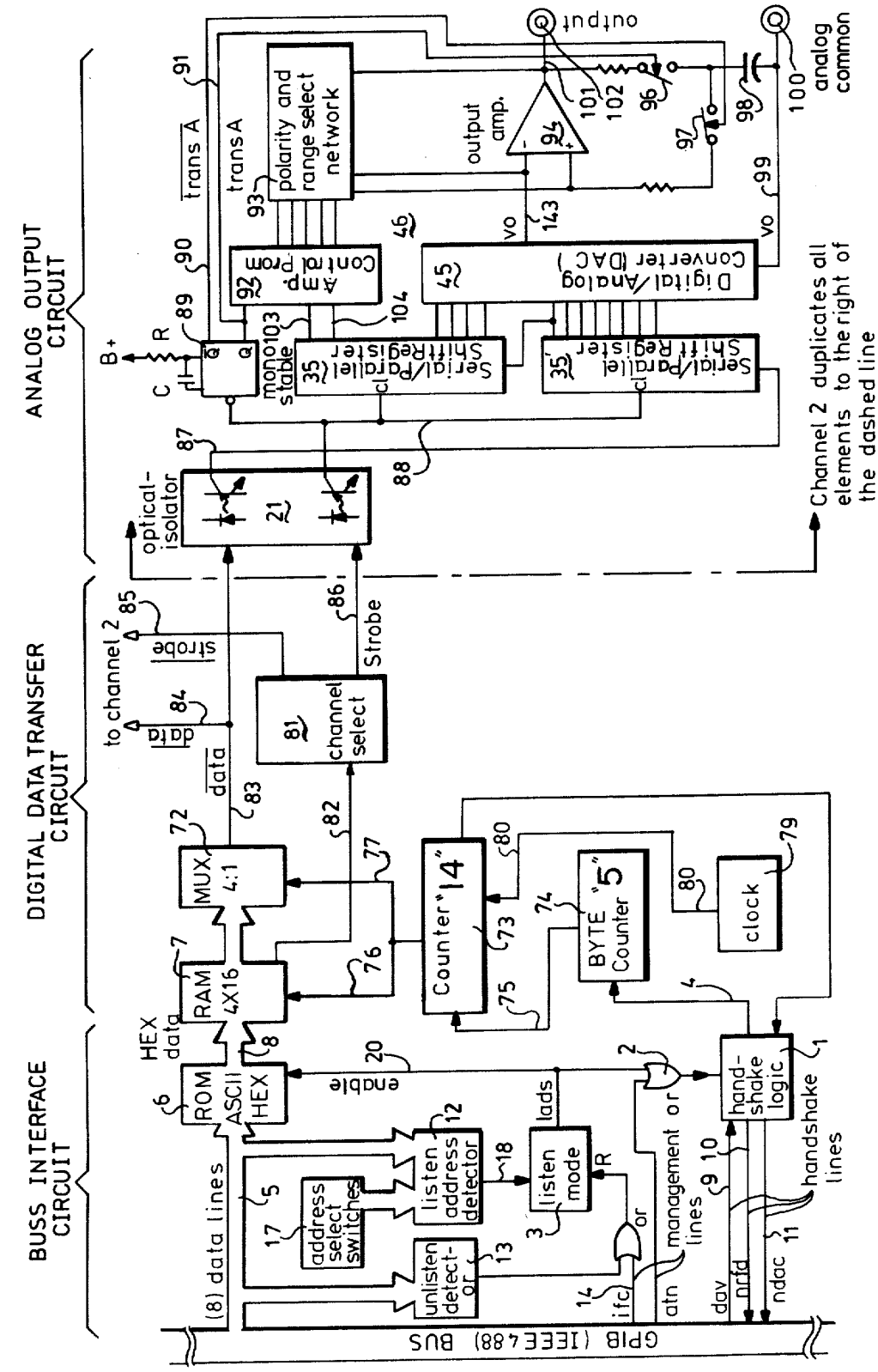

ANALOG OUTPUT CIRCUIT
DIGITAL DATA TRANSFER CIRCUIT
BUSS INTERFACE CIRCUIT
output
analog common
trans A
polarity and range select network
output amp.
Digital/Analog Converter (DAC)
Serial/Parallel Shift Register
monostable
optical-isolator
Channel 2 duplicates all elements to the right of the dashed line
to channel 2
strobe
data
channel select
MUX 4:1
RAM 4X16
HEX data
ROM ASCII HEX
Counter "14"
BYTE "5" Counter
clock
enable
lads
hand-shake logic
handshake lines
(8) data lines
address select switches
listen address detector
listen mode
unlisten detect-or
management lines
atn
ifc
dav
nrfd
ndac
GPIB (IEEE488) BUS

Fig.6

Fig.7

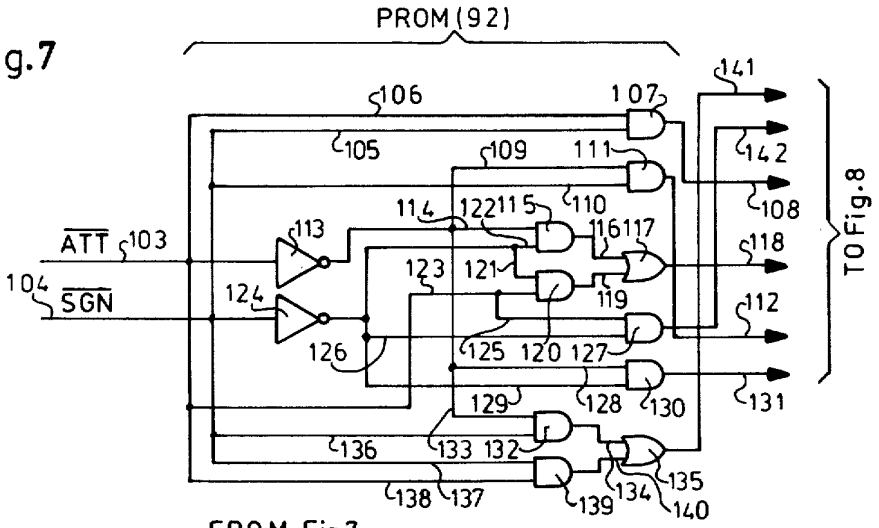


Fig.8

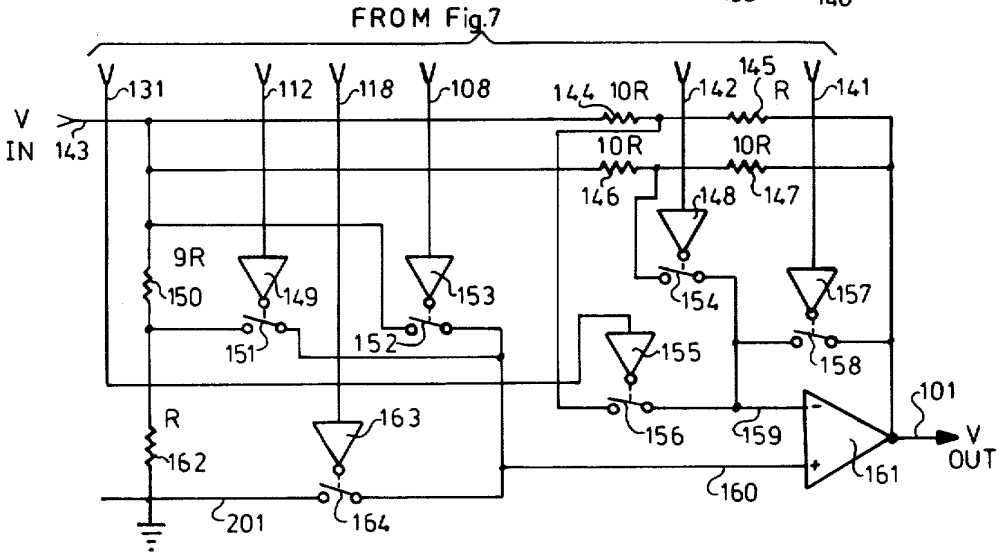


Fig.9

INPUT		SWITCH CONDITION						OUTPUT	
$\overline{ATT}$	$\overline{SGN}$	152	151	164	154	156	158	POL.	GAIN
0	0	OFF	OFF	ON	OFF	ON	OFF	—	X0.1
0	1	OFF	ON	OFF	OFF	OFF	ON	+	X0.1
1	0	OFF	OFF	ON	ON	OFF	OFF	—	X1.0
1	1	ON	OFF	OFF	OFF	OFF	ON	+	X1.0

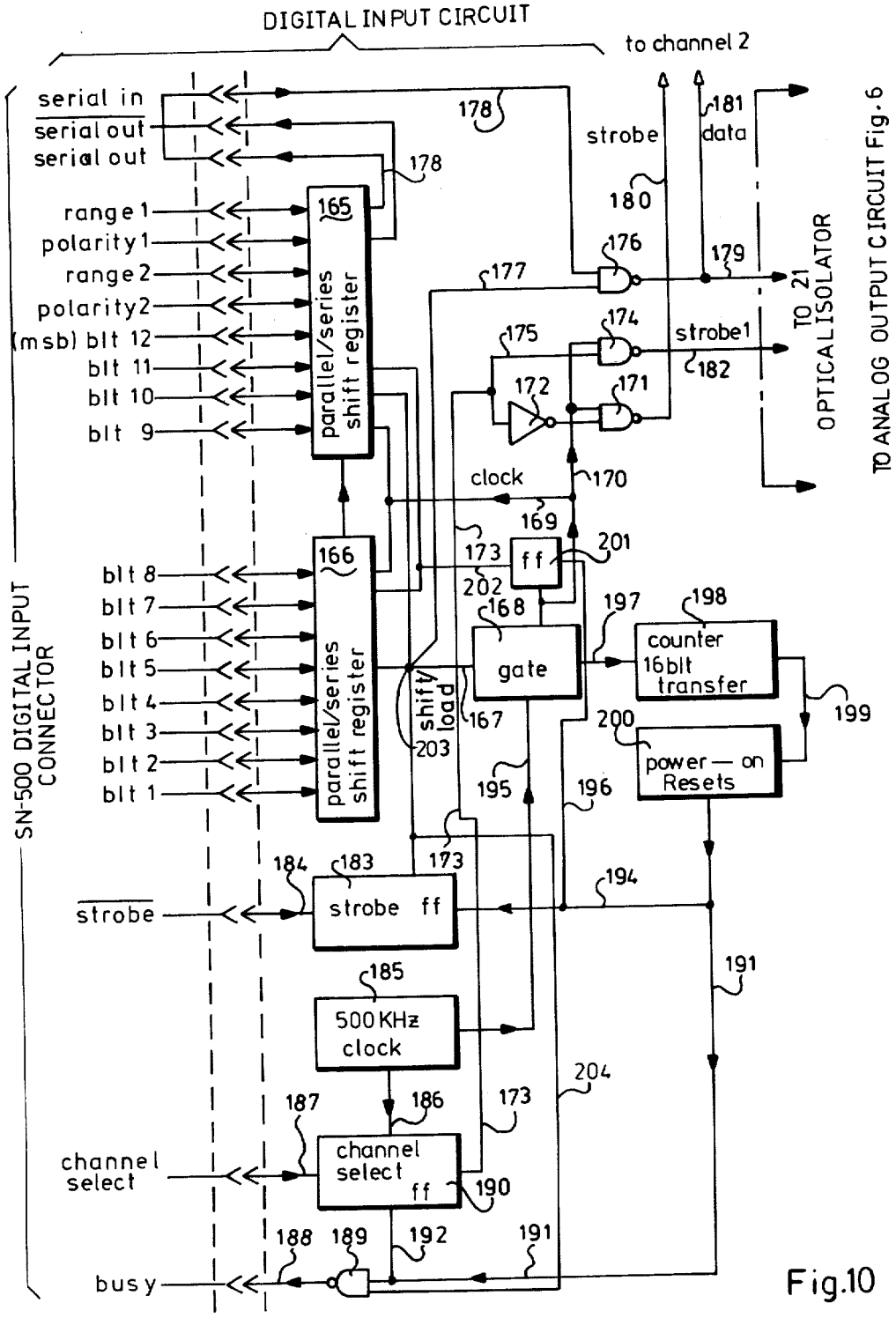

DIGITAL INPUT CIRCUIT
to channel 2
SN-500 DIGITAL INPUT CONNECTOR
serial in
serial out
serial out
range 1
polarity 1
range 2
polarity 2
(msb) bit 12
bit 11
bit 10
bit 9
bit 8
bit 7
bit 6
bit 5
bit 4
bit 3
bit 2
bit 1
parallel/series shift register
parallel/series shift register
strobe
busy
channel select
strobe ff
500 KHz clock
channel select ff
clock
shift/load
gate
ff
counter 16 bit transfer
power — on Resets
strobe
data
strobe1
TO 21 OPTICAL ISOLATOR
TO ANALOG OUTPUT CIRCUIT Fig. 6
165
166
167
168
169
170
171
172
173
174
175
176
177
178
179
180
181
182
183
184
185
186
187
188
189
190
191
192
194
195
196
197
198
199
200
201
202
203
204

Fig.10

SYSTEM FOR INTERFACING COMPUTERS WITH PROGRAMMABLE POWER SUPPLIES

PRIOR ART

U.S. Pat. No. 3,810,103 entitled "Data Transfer Control Apparatus" describes and claims a data transfer system which is described as follows in the "Abstract" of the Patent:

"An improved data transfer system enables a common data source to operate asynchronously with a plurality of different data receivers at a data transfer rate that is limited only by the operating rates of the data receivers and the data source. The operating conditions of the data receivers are sensed in common by the data source and the operating condition of the data source is sensed by the data receivers in order to optimize the data transfer rate without loss of data and with restriction to a predetermined (or synchronous) data transfer rate".

The above designated patent was assigned to Hewlett-Packard Co., of Palo Alto, Calif. and the system it describes has been accepted and is known as the IEEE or the HP-IB interface to be designated here below as the GP-IB (General Purpose Interface Bus).

In its standard form the GP-IB (Hewlett Packard Interface Bus) employs 16 lines to interconnect up to 15 instruments. Eight of these lines are used to transmit data and the remaining eight are used for communication timing (Handshake) and control. Data is transmitted as a series of eight-bit "bytes", normally using the seven-bit ASCII (American Standard Code for Information Interchange) plus an eighth bit available for parity checking. Data is transferred by an interlocked "handshake" technique permitting asynchronous communication over a wide range of data rates.

Communications between devices on the GP-IB bus system must be able to perform at least one of the functions designated as "Listener", "Talker" and "Controller". The "Listener" is a device capable of receiving data from other instruments as, for example, printers, programmable power supplies, display devices, programmable signal sources and the like. The "Talker" is a device capable of transmitting data to other instruments as, for example, tape readers, voltmeters putting out data, counters putting out data and the like. The "Controller" is a device capable of managing communications over the GP-IB as, for example, addressing and sending commands as from a calculator or computer with appropriate 1/O interfacing. Only one device at a time may act as an active talker although up to 14 devices may be simultaneous listeners and only one device at a time may be an active controller.

For further details reference is made to the publication entitled "Condensed Description of the Hewlett Packard Interface Bus part No. 95401-90030."

The Present Invention

In order to expand the usefulness of the GP-IB concept, the present invention provides a unique digital programming system which has the commercial designation SN-488 which designation will be used below for convenience in the disclosure. The SN-488 is intended for use in controlling voltage programmable power supplies and contains circuits for responding to listener mode of the GP-IB only. The SN-488 comprises two main components, first, an interface to operate between the GP-IB and an internal bus, and, second, a program card to operate between this internal bus and up to 8 programmable power supplies (16 functions). Thus, using only a single GP-IB bus connection (intended for controlling a single instrument) the SN-488 makes possible the control of up to 8 programmable power supplies which would otherwise require over half of the 15 connection capacity of the GP-IB.

The first stage of the SN-488, the interface, provides means responding to the handshake signals, listen and unlisten commands and converts the ASCII (8 line) input to hexadecimal byte-serial stored in a read only memory (ROM coupled to the internal bus of the SN-488. The second stage, the program card, recognizes a particular address, shifts the ROM stored data to a series of latches, followed by two digital to analog converters (DAC) which in turn provide programming analog voltages to the power supplies to be programmed. Along with the amplitude commands are range and polarity commands (bytes) which are also processed in the same manner to provide range and polarity control signals in the latches and thence to the programmed power supplies.

In the preferred form of the invention the programmable amplifiers operated in sample and hold mode make possible a substantial simplification of the overall circuitry and, in particular, the elimination of the second memory i.e the latches.

In the drawing:

FIG. **1** is a block diagram illustrating the bus structure and interface connections of GP-IB. (Prior Art).

FIG. **2** is a block diagram of the SN-488 programming functions connected between the GP-IB and the internal bus.

FIG. **3** is a block diagram of the SN-488 programming card which functions between the internal bus and the programmable power supplies to be controlled.

FIG. **4** is a diagram partly schematic and partly block illustrating a single channel of a programmable power supply, connected as a current regulator.

FIG. **5** is a diagram partly schematic and partly block illustrating two channel control of a programmable power supply.

FIG. **6** is a block diagram of the preferred form of the present invention.

FIG. **6A** is a block representation of how information is stored in a temporary memory in FIG. **6**.

FIG. **7** is a block diagram of inverters and gates useful in explaining the functioning of PROM **92** of FIG. **6**.

FIG. **8** is a block diagram of the polarity and range select network **93** and programmable amplifier **94** of FIG. **6**.

FIG. **9** is a Truth Table useful in explaining the functioning of PROM **92** of FIG. **6** (detailed in FIG. **7**) and the programmable amplifier as detailed in FIG. **8**.

FIG. **10** is a block diagram of a form of the invention useful for utilizing parallel input data.

FIG. **1** is a block diagram showing the GP-IB bus structure comprising eight dedicated lines plus an eight line data bus. The dedicated lines are designated in two groups. The first group of three lines are designated as "handshake" lines and the second group of five lines as "control" lines. The three handshake lines include DAV, data valid; NRFD, not ready for data; and NDAC, no data accepted. Of the five control lines, only two are used in the present invention, namely, ATN, attention and IFC, interface clear. The SN-488 system of the present invention has no talk-back provisions and

hence has no need for the other lines, SRQ, REN and EOI. To illustrate typical applications of the GP-IB, four devices are shown connected to the bus. The first device designated "A" is able to "talk", "listen" and "control" such as a calculator. The second device designated "B" is able to "talk" and "listen" as, for example, a digital voltmeter. The third device designated "C" is only able to "listen" as, for example a signal generator. The fourth device designated "D" is only able to "talk" as, for example, a tape recorder. In the system of the present invention, devices that listen only (C) are to be discussed.

FIG. **2** is a block diagram of the essential components interconnecting the GP-IB and the SN-488 internal bus in accordance with the present invention. The handshake logic **1** accepts inputs from ATN (attention) or listen mode **3** through OR gate **2** and DAV (data available) over line **9**. Handshake logic **1** replies NRFD (not ready for data), NDAC (data not accepted) over lines **10** and **11** respectively and strobes the internal bus **7** over line **4**. Reference is again made to Hewlett-Packard Condensed Description Part No. 59401-90030 for further details of the handshake process and its operation.

FIG. **2** includes two decoding devices, namely, listen address detector **12** and unlisten detector **13** both coupled to the data lines. There are two occurrences which are used to clear the interface, one an IFC signal over line **14** and the other an unlisten coded signal over the data lines **5** actuating unlisten detector **13**. The two unlisten signals are OR gated through OR gate **15** and applied to listen mode control **3** over line **16** to clear any response being processed. The listen address detector **12** is set to respond to a predetermined coded signal from the data lines by means of address select switches **17** which are manually operated switches set to accept or decode a predetermined coded data signal for a particular piece of equipment to be programmed. The listen address detector **12** upon receiving its address signal, outputs over line **18** to listen mode control **3** which in turn signals handshake logic **1** over lines **19-20** and enables ROM **6**. The ROM **6** is an ASCII to HEX code converter which is required here since the data lines carry ASCII coded signals while the system of the present invention is designed to use HEX coded signals.

It can be seen from the above that the present invention uses the three handshake lines (DAV,NRFD and NDAC), two control lines (IFC and ATN) and the eight data lines. The other three control lines are not required for the listener mode only of the present invention.

FIG. **3** is a block diagram of the interface between the internal bus **7** (see FIG. **2**) and the programmable amplifiers and power supplies being controlled. The data (byte serial hex) from internal bus **7** is applied to a series of opto-isolators **21** over lines **22**. Control logic **23** accepts control signals MCA over line **24** when the data on lines **22** contain the address set in address select **25** is detected in card address detector **26** and applied over lines **27**. Control logic **23** also receives from internal bus **7** the strobe over line **28** and the ASCII signal designated as the equals sign over line **29**. The ASCII character "=" received over the GPIB bus is decoded by the PROM **6** and applied over line **29** to the control logic **23**. It is used as a delimiter in the data string to separate the card address information from the actual data. The control logic **23** in response to its inputs enumerated above provides two control signals over lines **30** and **31**, coupled in opto-isolator **21** to provide a shift signal on line **32** and a latch signal on line **33**. The otpo-isolators **21** merely provide optical isolated coupling between lines **22** and **34** as well as **30-32** and **31-33** mentioned above. The isolated data signals from lines **22** appearing on lines **34** are applied to shift register **35** where they are stored and accumulated until a complete complement of signals have been received and a latch signal on line **33** latches the accumulated data (control) signals to latches **37** over lines **36**. The signals thus applied are held in latches **37** and applied to digital-to-analog-converters (DAC) **38** and **39** over lines **40** and **41** respectively where analog control voltages are generated in accordance with the applied digital data. The range and *polarity* signals are applied to lines **42** and **72**. The control voltages from DACs **40** and **41** are modified in two programmable amplifiers **44** and **46** by the range and polarity bits over lines **42** and **72** to provide analog voltages for controlling programmable power supplies **49** and **50** over lines **47** and **48** respectively.

FIGS. **4** and **5** are simplified block diagrams of two typical programmable power supplies adapted to be controlled in accordance with the present invention as described above. The power supply of FIG. **4** comprises the well known combination of an error amplifier controlling current from an unregulated source **52** by means of a pass transistor **53** into a load **54**. Load current is sensed across resistor **55** and the sensed voltages is fed back over line **56** and through adjustable current control resistor **57** to null junction **58** connected to input terminal **59** of operational (error) amplifier **51**. While three lines **47, 48** and common are provided from the control amplifiers **44** and **46** (FIG. **3**) only two are used in this case. Line **60** is the common line going to common point **64** of the power supply. Line **62** is not used, and line **61** carrying analog voltage control signals is connected through source resistor **63** to null junction **58**. The equation relating the control voltage, load current, input and current control resistors is as follows:

$$\frac{\text{control voltage}}{\text{current sensed voltage}} = \frac{R_{63}}{R_{57}}$$

Typical values are as follows:
control voltage = 10 volts
current sensed voltage = 1 volt
R_{63} = 10,000 ohms
R_{57} = 1,000 ohms
R_{55} = 1 ohm
Using these constants the load current will be:

$$\text{current sensed voltage} = R_{55} \times I_L \text{ (load current)}$$

$$\text{Then } I_L = \frac{10 \times 1000}{1 \times 10{,}000} = 1 \text{ ampere}$$

The load current is obviously 1 ampere per thousand of current control resistance.

$$I_L = \frac{10\,R_{57}}{10{,}000} = \frac{R_{57}}{1{,}000} \text{ Amperes}$$

FIG. **5** is a simplified block diagram of a programmable voltage regulated power supply with controlled current limiting. The basic error amplifier, unregulated voltage source, pass transistor, current sensing resistor

and load are as in FIG. 4 and bear the same numerals. However, this is basically a voltage regulated power supply and the feedback line 70 is connected to the high side of the load and through adjustable voltage control resistor 71 to junction point 58. Line 61 from the control circuits is connected through resistor to junction point 58. The well known relationship in this voltage regulated power supply is as follows:

$$\text{Load voltage} = \frac{R_{71}}{R_{63}} x \cdot \text{control voltage}$$

The control voltage is supplied over line 61 (contained in lines 48) from programmable amplifier 44 (FIG. 3). Common line 60 is connected to common point 65. This power supply is provided with a second error amplifier 66 which is connected to provide a limiting action when the load current tends to exceed a predetermined value. The voltage drop in current sensing resistor 55 is compared with a control voltage over line 62 (from amplifier 44) at the input to error amplifier 66. The pass transistor 53 is controlled by signals applied to its base over line 69. In the absence of over current the error amplifier 51 acts through diode 68 to control the pass transistor in accordance with the above equation for load voltage. However, if amplifier 66 receives an input from current sensing resistor 55 which exceeds its control voltage over line 62, its output tends to go low acting through diode 67 to hold down the voltages on line 69 and controlling pass transistor 53 to cease from response to output from error amplifier 51.

The invention as described above is the basis of the preferred form of the invention as shown in FIG. 6, and described in detail below. The programmable amplifier shown in FIGS. 7 and 8 and described below is used in both forms of the invention. The discovery that the programmable amplifier makes possible the simplification led to the preferred form of the invention.

FIG. 6 is a block diagram of the preferred form of the present invention. Brackets at the top of the diagram divide the circuit into three functional ports, namely; "Bus Interface Circuit", "Digital Data Transfer Circuit" and "Analog Output Circuit". The Bus Interface Circuit has been described above being the subject of FIG. 2 and the Analog Output Circuits are the circuits of FIG. 3 to the right of and including the opto-isolators 21 also described above except for the omission of latches 32 which will be described more fully below.

As described in connection with FIG. 2 above, the information on data lines 5 is in ASC11 code and is converted to HEX (hexadecimal) in ROM 6. This converted data is fed to RAM (random access memory) 7 over four lines 8. This RAM is a so called 4×16 temporary memory in other words it has a capacity of 16 "words" 4 bits per word although its full capacity is not required at this point it it chosen for the job since it is the lowest capacity standard commercial product for the purpose. Actually only five 4 bit words are required as illustrated in FIG. 6A. The first word or byte carries the channel select information (CH) and may call, in this case, for channel 1 or channel 2. The next byte carries the phase and range or multiplier information (P & R). The next three bytes twelve bits of data carrying information as to the voltage value to be programmed. Byte counter 74 coupled to handshake logic 1 over channel 4 controls counter 73 over channel 75 while counter 73 counts 14 i.e. 2 counts for P&R and 12 counts for data. The output of counter 73 over lines 76 and 77 controls RAM 7 to transfer the stored HEX information over lines 78 to multiplexer (MUX 4:1) 72 which in turn serializes data over line 83 to optical isolator 21 and over line 84 to the second channel. Channel selector 81 receiving a signal from ROM 7 over line 82 strobes optical-isolator 21 if channel 1 has been selected or over line 85 to optical-isolator of channel 2 if it has been selected.

As described above in connection with FIG. 3 data is passed on by optical-isolators 21 to shift registers 34 which accumulate the data. In order to clarify the functioning of the Analog Output Circuits of FIG. 6 the operation of the programmable amplifier (46) including PROM 92, polarity and range select network 93 and operational amplifier 94 will be described as shown in FIGS. 7 and 8.

FIGS. 7 and 8 are detailed block diagrams explaining the operation of the following components of FIG. 6 including; the programmable/sample and hold output amplifier 94 (FIG. 6); the polarity and range select network 93 (FIG. 6); the amplifier control PROM 92 and associated switches in which the programmable output amplifier 94 is operated as a sample and hold amplifier thereby eliminating the necessity of supplying the latches shown in FIG. 3 and described above. In order to clarify the explanation, the PROM 92 equivalent is shown in the form of a plurality of inverters and gates. FIG. 9 is a Truth Table explaining the operation of the inverters and switches of FIG. 8.

FIGS. 7, 8, and 9 are taken together. Two input lines 103 and 104 designated $\overline{\text{ATT}}$ and $\overline{\text{SGN}}$ respectively control the output functions of gain and polarity (POL). The inverters and gates of FIG. 7 convert the four possible input conditions of lines 103 and 104 to actuate switches 152, 151, 164, 154, 156 and 158 as shown in the Truth Table of FIG. 9 and the resulting output conditions.

FIG. 7 will be described below and provides the predetermined switching conditions which are alternately provided by PROM 92 as shown in the Truth Table of FIG. 9. Taking the switches one at a time; line 108 to switch 152 is ON when both lines 106 and 105 to AND gate 107 are 1 (high); line 112 to switch 151 is ON when line 109 as inverted by inverter 113 is 1 and line 110 is 1 turning on AND gate 111; line 118 to switch 164 is ON when lines 114 and 122 as inverted by inverters 113 and 124 turn on AND gate 115 and hence over line 116 to OR gate 117 making line 118 a 1 or when line 123 and line 121 inverted by inverter 124 are both ON causing AND gate 120 to place a 1 on line 119 and thus through OR gate 117 a 1 on line 118; line 142 to switch 154 is ON when line 125 is 1 and line 126 as inverted by inverter 124 is 1 turning on AND gate 127; line 131 to switch 156 is ON when lines 128 and 129 inverted by inverters 113 and 124 respectively are 1 turning on AND gate 130; and line 141 to switch 158 is ON when line 133 inverted by inverter 113 and line 136 are on turning on AND gate 132 placing a 1 on line 134 and through OR gate 135 to line 141 or when line 137 and line 138 are both ON causing AND gate 139 to place a 1 on line 140 and through OR gate 135 to line 141. The inverter symbols 149, 153, 148, 157, 155, 157 and 163 are to be taken as the drivers of switches 151, 152, 154, 157, 158 and 164 respectively.

With the description of FIG. 7 as given above and Truth Table of FIG. 9, the functioning of the various switch combinations as shown in FIG. 8 will now be

described. When both input lines **103** and **104** (see FIG. 7) are at logic 0, switches **164** and **156** are closed and the others are open. Switch **164** connects the non-inverting input **160** of amplifier **161** to common line **201** and switch **156** connects inverting input **159** of amplifier **161** to the junction between feedback resistors **144** and **145**. Resistors **145**, **144**, **150** and **162** are labeled R, **9R** or **10R** indicating their relative values. Thus, with an analog input on line **143** applied to one end of resistor **144** and a feedback ratio of R/10R the input on line **144** is divided by 10 so that the gain as shown in the OUTPUT table is 0.1. Since the input is in effect to the inverting input of amplifier **161**, the polarity (POL) of the output on line **101** is negative. To reiterate, 0—0 on input lines **103** and **104** provide a negative output multiplied by 0.1 with respect to the analog signal on input line **143**.

To continue, a logic 0 on input line **103** and a logic 1 on input line **104** processed by the inverters and gates of FIG. 7 provide outputs on lines **112** and **141** closing switches **151** and **158**. Switch **151** places the analog from line **143** divided by 10 on non-inverting input **160** and switch **158** connects output line **101** to inverting input **159** so that the input appears on output line **101** multiplied by 0.1 and of the same polarity (+).

Next, if logic 1 is applied to input line **103** and logic 0 to input line **104**, the inverters and gates of FIG. 7 actuate switches **164** and **154**. Switch **164** connects non-inverting input **160** to common line **201** and inverting input **159** to the junction between the two equal resistors **147** and **146**. Resistor **147** is also connected to output line **101** acting as a feedback resistor and resistor **146** is connected to analog input line **143**. Thus, with equal input and feedback resistors the gain from input line **143** to output line **31** is 1. The input being applied to the inverting input **159** causes the output on line **101** to be inverted (−). Thus, the output is negative at a gain of 1 with respect to the analog input signal on line **143**.

Finally, the fourth possible condition is with both input lines **103** and **104** at logic 1 and programmed by the inverters and gates of FIG. 7 closing switches **152** and **158**. Switch **152** places the full analog input of line **143** on the non-inverting input **160** providing a non-inverted output on line **101** and switch **158** connects output line **101** to inverting input **159** for a gain of 1. Thus, the output is positive (+) at a gain factor of 1.

The analog switches described above are preferrably solid state switches such as the Siliconix type DG201 or their equivalent.

Solid state switches have several differences when compared with mechanical or electro-mechanical switches. For example, they are much faster, and take less power to operate but, on the other hand, they have significant series resistance when closed. In order for this impedance to be tolerated and not cause errors in the circuits of the present invention, the switches are placed, in all but one instance, in series with the input to the operational amplifier **161**. Since the inputs are both high impedance, of the order of megohms, the switch impedances, of the order of a few hundred ohms at most, no appreciable errors are introduced by their use. In one case switch **158** connects output to input of amplifier **161** but without any other input connection, the amplifier will exhibit unity gain from its non-inverting input even with some feedback impedance.

Returning to FIG. **6** after having explained the operation of the programmable amplifier in connection with FIGS. 7 and **8** it is appropriate to return to FIG. **6** with an explanation of the remaining details of the Analog Output Circuit. Output amplifier **94** (programmable as described above) is operated as a sample and hold amplifier. In the hold mode switches **97** and **95** are closed causing amplifier **94** to operate at unity gain repeating the voltage held in capacitor **98** to output terminal **102** over line **101**. In order to provide a new output in response to data accumulated in shift registers **35**, switch **97** is opened and switch **96** is closed thereby charging capacitor **98** to the new data value. The switching between the sample and hold conditions is controlled by retriggerable monostable multivibrator **89** over lines **90** and **91** respectively. With no data being received from the optical-isolators **87**, no signal is provided on line **88** to the multivibrator **89** and its Q output remains high holding switch **96** closed, and thereby sampling the previously stored data in shift registers **35** and outputting it. The instant a new data bit is supplied through the optical-isolators **21** which will add up to a new command, the first bit over line **88** causes monostable **89** to trigger, switching its output from Q to $\overline{Q}$ and closing switch **96** and opening switch **97**. The output on terminal **102** is thus held by the sampled charge on capacitor **98** until monostable **89** returns to its initial condition. Now, monostable **89** is provided with a time delay in the form of resistor R and capacitor C so that when it is switched by a data bit it stays switched for a predetermined interval. This interval is made longer than the periods of the data bits so that once a data string is started monostable **89** switches and remains so until a short time after the data string has ended. Once it ends, monostable **89** switches back opening switch **97** and closing switch **96** to provide a new output in accordance with the new data string. In this way the need for the latches **37** are shown in FIG. **3** is eliminated thereby decreasing the cost and increasing the reliability of the system.

Additional details of the sample and hold amplifier operation will be found in U.S. Pat. No. 4,209,753.

FIG. **10** shows a modified form of the present invention adapted to receive parallel input data and commands. This form of the invention does not require the Bus Interface Circuit shown and described above but only a Digital Input Circuit and the Analog Output Circuit. The Analog Output Circuit is identical with the circuit of the same designation shown in FIGS. **6**, **7** and **8** and described in detail above. The Digital Input Circuit is adapted to receive parallel input data and commands, to serialize this data and to pass the serialized data on to the Analog Output Circuits as described in detail below.

The two parallel to series shift registers **165** and **166** receiver parallel input commands and data over sixteen input lines, eight to each register designated as range **1**, polarity **1**, range **2**, polarity **2** and bits **1** through **12**. The serialized commands and data flow out of the upper shift register over line **178** to NAND gate **176**. When gate is opened, as will be described below, the commands and serialized data flows over line **178** (channel **1**) or **181** (channel **2**) to the Analog Output Circuit under the timing control of 500 KHz clock **185**. The timing pulses from clock **185** are applied over lead **186** to channel select flip-flop (ff) **190** and to gate **168** over lead **195**.

Operation of the system is initialized by reset **200** which applies a pulse to busy NAND gate **189** over line **191** signaling non-busy to busy line **188**; resetting strobe flip-flop **183** to place strobe line **184** in receptive condition and flip-flop **201** to inhibit read out of registers **165**

and **166** over line **202**. With these conditions set up shift registers **165** and **166** may receive their parallel input commands and data. In the absence of a strobe signal on input **184**, strobe flip-flop **183** applies an inhibit signal to junction **203** closing gate **168** over line **167**, permits loading of registers **165** and **166** and closes data gate **176** over line **177** and blocks clock signals over input line **195** to gates **171** and **174** over line **170** and clock signals to registers **165** and **166** over line **169**. Under these conditions parallel input signals to register **165** and **166** may be received but no strobe can pass through gates **171** or **174** and no data can pass through gate **176**. During data loading a channel select signal designating either channel **1** or channel **2** is applied to channel flip-flop **190** over input line **187**.

Once data has been loaded into registers **165** and **166** the system is ready for the serial read out. This read out is initiated by applying a strobe pulse to strobe flip-flop **183** over line **184** which in turn changes the condition at junction point **203** which in turn unblocks gates **168** and **176**. The leading edge of the first clock pulse following this unblocking of gate **168** passing clock pulses to open strobe gates **171** or **174** depending on which channel has been selected and releases flip-flop **201** permitting clock pulses to read out registers **165** and **166** at the trailing edges of the clock pulses. At the same time counting is started in counter **198**.

Now, under these conditions serial data is clocked by the trailing edges of the clock pulses out of registers **165** and **166** over line **178**, through gate **176** and over line **179** to the analog output circuits, optical isolator **21**, etc. to complete the control and application of data to the output devices being controlled (as described in connection with FIGS. **7**, **8** and **9** above).

As can be seen there are 16 input lines carrying commands and data into registers **165** and **166**. In other words these registers when filled can hold up to 16 bits of information. Accordingly they will be emptied when 16 bits are read out serially. This reading out is monitored by 16 bit counter **198** which fills at the 16th count. At the 16th count this counter sends a pulse over line **199** to reset **200** which in turn returns strobe flip-flop **183** to its initial condition over line **194** and opens busy gate **189** over line **191**. The system is now ready to receive and process the next set of commands and data repeating the sequence described above.

While the preferred form and modified forms of the present invention have been shown and described, further modifications are possible within the spirit and scope of the invention which is set forth in particular in the appended claims.

I claim:

1. In a digital information interfacing system for utilizing data bytes from a plurality of data lines to provide analog voltage control of voltage/current programmable power supplies, the combination of;

means coupled to said data lines for temporary storage of said data bytes received from said data lines to provide stored data bytes;

means coupled to said data lines and said temporary storage means for controlling a predetermined number of bytes being accepted by said temporary storage means;

means coupled to said temporary storage means for serializing said stored data bytes;

means for passing said serialized data bytes through optical isolation means to provide isolated data;

means including a series to parallel shift register for converting said serial isolated data to parallel form;

means including a digital to analog converter for converting said parallel data to analog form;

means responsive to said analog form data for generating an analog voltage;

and means for using said analog voltage to control said programmable power supplies.

2. A digital information interfacing system as set forth in claim **1**, and

wherein said temporary storage means comprises a random access memory (RAM).

3. In a digital interfacing system for utilizing data bits from a plurality of data lines to provide analog control voltage for the control of voltage/current programmable power supplies, the combination of;

parallel to series shift register coupled to said data lines for temporary storage of said digital data bits received from said data lines to provide temporarily stored digital data bits;

means coupled to said data lines and said parallel to series shift register for controlling a predetermined number of bits being accepted by said parallel to series shift register;

means connected to said shift register for passing the output of said register in series through optical isolation means to provide isolated digital data bits;

means including series to parallel shift register means for converting said serial isolated data bits to parallel form;

means including a digital to analog converter for converting said parallel data to analog form;

means responsive to said analog form data for generating an analog voltage;

and means for using said analog voltage to control said programmable power supplies.

* * * * *